Asynchronous SAR ADC with self-timed track-and-hold

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This paper presents an asynchronous SAR ADC featuring a self-timed track-and-hold (STH) architecture. The design aims to address the common timing issue of divider-based clock generation, where the fixed-time track-and-hold (FTH) period often results in incomplete conversions due to prolonged conversion times time due to comparator metastability. To alleviate the degradation of the ENOB induced by these delays, the proposed STH method is introduced so that more conversion period is secured without requiring a high-speed input clock. Based on measurements, the proposed STH method achieves up to 0.7 bit improvement over the conventional FTH approach as conversion time increases.

Introduction: SAR ADCs are widely used due to their medium-to-high resolution, low power consumption, and compact size [1–4]. Conventional asynchronous topology enables faster operation by the self-timed mechanisms [5–8], as shown in Figure 1a. These mechanisms comprise track-and-hold (T/H) and conversion periods [4], with the endpoint of each conversion dynamically determined for every sampling instance [5–8]. Typical asynchronous architectures require a high-frequency input clock to generate a predetermined T/H period [9, 10], and each clock cycle also needs a margin to account for clock jitter [11]. To alleviate speed limitations, alternative techniques like tapered clock generation are available [12]. For instance, to achieve a 25% T/H duty cycle, the input clock needs to be four times faster than the sampling clock frequency (fs). It is challenging to generate optimal T/H periods because faster input clocks are required to generate accurately controlled periods. Additionally, the asynchronous SAR ADC may lose LSB conversions because of longer decision time in comparators' metastability, as shown in Figure 1b [13]. This paper presents a sampling clock generation without requiring higher input clock frequency and increases the timing margin in LSB conversions with a self-timed clocking scheme.

Proposed architecture: Figure 2a shows illustrates the overall SAR ADC configuration, incorporating both the traditional FTH and our proposed STH modes. For example, the FTH method utilizes a clock that is four times faster to generate a T/H with a 25% duty cycle. As a result, to match the sample rate of the proposed STH method, FTH requires a four times faster clock. In the conventional clock generation scheme, *EOC* conversion must happen before the T/H starts as shown in Figure 1a otherwise the LSB conversion data is lost as shown in Figure 1b.

The STH mode operates through a variable T/H clock ($CK_{T/H,var}$) generation, as shown in Figure 2b. After the LSB conversion completes, either D_{OP}<0> or D_{ON}<0> becomes high. This transition generates an *EOC* signal two clock-to-Q delays later. The high state of *EOC* then triggers an additional clock pulse known as *valid* as shown in Figure 2b. This *valid* activates $CK_{T/H,var}$ to high after one cycle comparator clock delay, so that the longer conversion time is secured in the case of longer decision time in comparators. When the external clock (CK_{EXT}) transitions to zero, both *EOC* and $CK_{T/H,var}$ are reset to zero as shown in Figure 2c. Even if the OR gate enters a metastable state, the system effectively mitigates this issue by delaying the start of the next T/H cycle to obtain more time to resolve. The extra circuitry may introduce some delay, but the ability to dynamically adjust the T/H period for the next cycle could actually make the system faster. Metastability mainly occurs during LSB conversions due to small input differences. Nevertheless, the STH method can yield improvements of more than 1 LSB in the case of a large T/H period design.

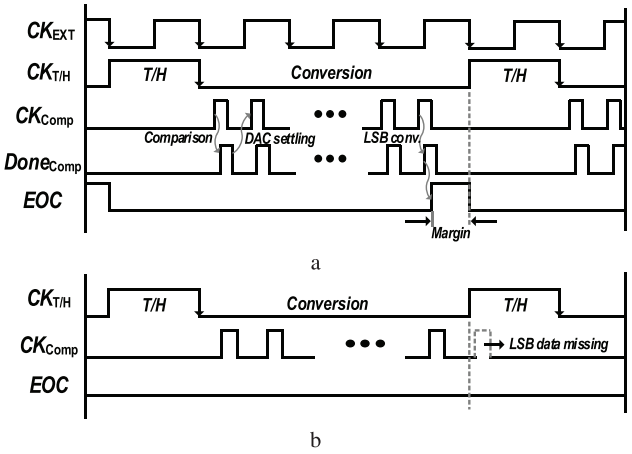

Fig. 1 *Timing diagram of the asynchronous SAR ADC*

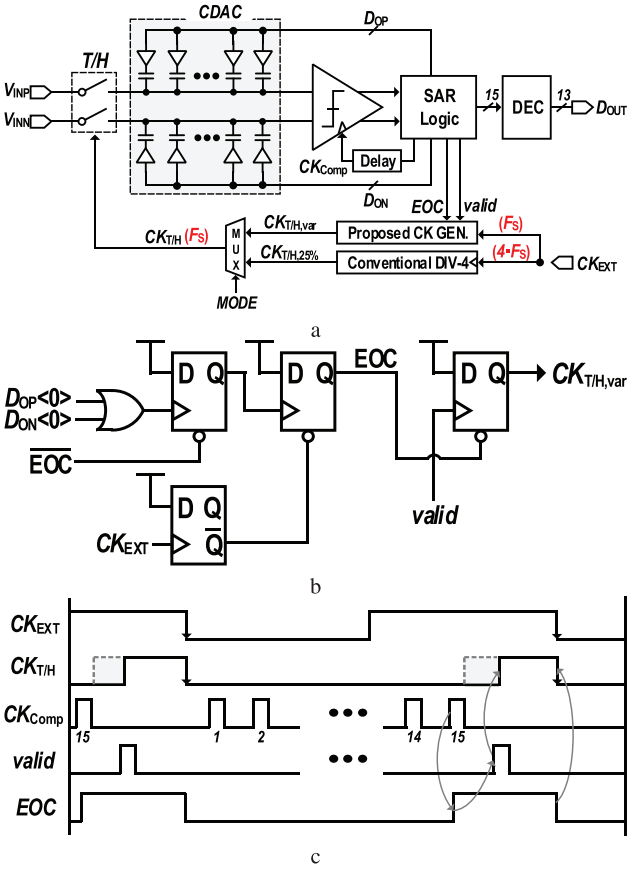

Fig. 2 *Proposed asynchronous SAR ADC*

Figure 3 shows simulated waveforms. Figure 3a displays T/H clock overlap due to various delay codes, simulating different conversion times. Unlike FTH, STH adjusts its T/H period based on conversion end times. Figure 3b demonstrates that STH successfully tracks input signals (VINP and VINN) even with a duty ratio below 25%, contrasting with FTH's divide-by-four period. As a result, STH maintains all conversion data while FTH loses one LSB. However, STH faces challenges in Region C due to insufficient tracking time.

Measurement result: The proposed SAR ADC, fabricated using a 55-nm ULP CMOS process, operates at a sampling rate of 1MS/s and achieves a Figure of Merit (FoM) of 19.59 fJ/conv-step. Figure 4 displays the die photograph of the ADC. The active area of the ADC measures 0.099 mm^2, with a power consumption of 43μW under a 1.2V supply voltage. This ADC performs 13-bit conversions with 15 total conversion cycles, of which two bits are used for redundancy. ADC employs a unit capacitor of 0.5 fF with MoM structure capacitors and features a two-stage dynamic comparator with a pre-amplifier and a cross-coupled

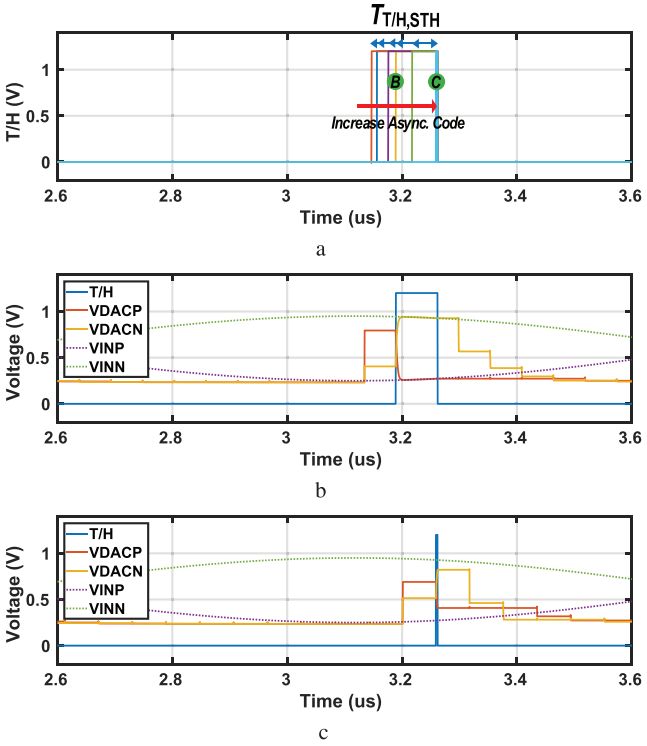

Fig. 3 *Simulation waveform of the proposed STH*

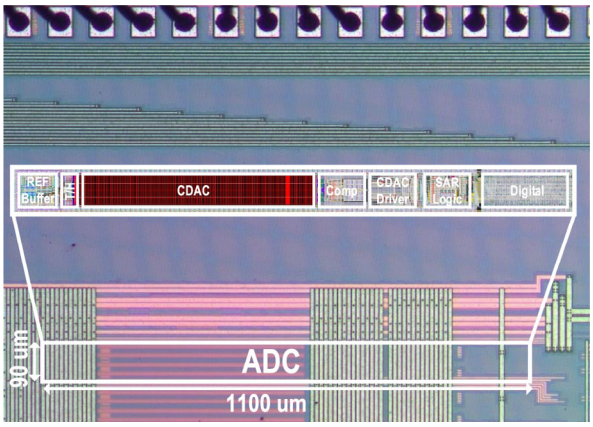

Fig. 4 *Chip photograph*

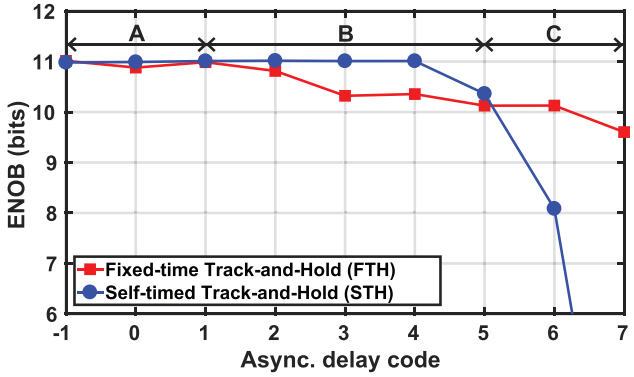

Fig. 5 *Measured ENOB according to asynchronous delay code*

latch step [1]. The delay cell for asynchronous clock generation has a delay step of approximately 800 ps and controls the DAC settling delay for ENOB performance comparison. The full-scale signal amplitude is applied as 0.8 V_{pp} centered around a common-mode voltage $V_{CM} = 0.6$ V.

Figure 5 shows the measured ENOB of FTH and STH as conversion period is increased by controlling delay code, and there are three regions according to performance. Region A indicates that all the conversions performed with sufficient timing margins, resulting in similar ENOB performance for FTH and STH. Region B shows a situation in which the decision time is increased, and the timing margin becomes gradually insufficient in existing FTH methods. This results in a loss of LSB data and poor ENOB performance in traditional FTH methods. On the other hand, the proposed STH borrows the conversion time from the T/H period in the next sample, so there is no performance degradation. Region C has an excessively short T/H period in the proposed TH scheme, resulting in resulting in rapid performance degradation. Therefore, to avoid such performance degradation in Region C, the minimum T/H period must be secured.

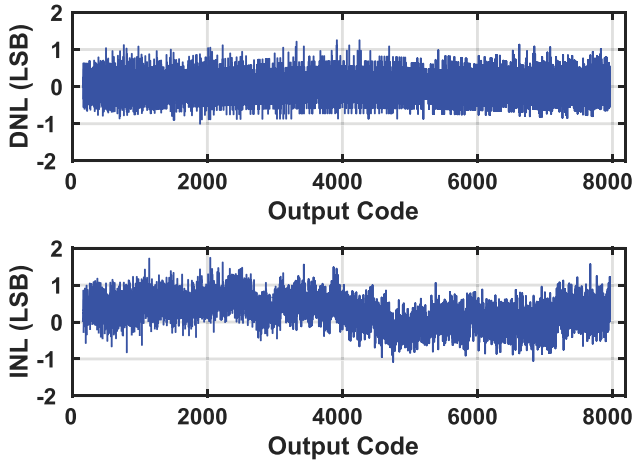

Fig. 6 *Measured DNL/INL of the proposed self-timed T/H*

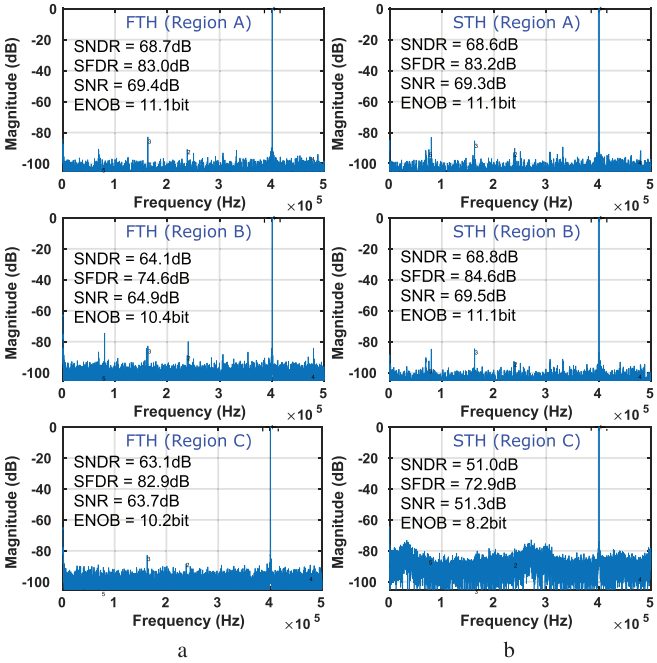

Fig. 7 *Measured FFT with FTH and STH*

Table 1. Measured performance of FTH and STH modes

	Conventional FTH	Proposed STH
ENOB [bit]	10.4	11.1
SNDR [dB]	64.1	68.8
SFDR [dB]	74.6	84.6

Figure 6 shows the DNL/INL performance of +1.2/-1.0 and +1.7/-1.1 LSB. Figure 7 shows measured six different FFT results obtained under varying delay codes, indicating that in Region B, the ENOB for FTH declines by 0.7 bits due to insufficient conversion time, while STH maintains an ENOB of 11.1 bits. Table 1 summarizes the comparisons of

Table 2. Performance comparison with the SAR ADCs

	This Work	[14]	[15]	[16]
Technology [nm]	55	40	65	110
Supply voltage [V]	1.2	1.1	0.85	0.9
Sample rate [MS/s]	1.0	1.0	1.0	1.0
Resolution [bits]	13	12	13	12
SNDR [dB]	68.8	68.1	66.4	68.3
SFDR [dB]	84.6	100.4	85.2	82.0
ENOB [bit]	11.1	10.77	10.4	11.05
DNL [LSB]	0.83	-	-	0.29
INL [LSB]	1.89	1.8@16b	-	0.55
Area [mm^2]	0.099	0.073	0.027	0.079
Power [μW]	43	31.1	45.2	24
FoM [fJ/conv.-step]	19.59	15	34.64	11.7

ENOB, SNDR, and SFDR under a delay code of 4, assuming Region B. The overall performance for the SAR ADCs are summarized in Table 2.

Conclusion: This paper introduces a simple and effective STH method that enhances the timing margin for the conversion period without needing a high-speed input clock. When compared to the traditional FTH method with the proposed method, the proposed variable method consistently yields superior ENOB performance across a longer range of conversion periods.

Author contributions: Sunghyun Bae: Conceptualization, data curation, formal analysis, investigation, methodology, visualization, writing - original draft, writing - review and editing. Sewon Lee: Data curation, resources. Siheon Seong: Data curation, resources. Jiwon Woo: Data curation, resources. Minjae Lee: Supervision.

Acknowledgements: This work was supported by the the Commercializations Promotion Agency for R&D Outcomes (COMPA) grant funded by the Korea Government (MSIT) (No. 2021I500). The EDA Tool was supported by the IC Design Education Center (IDEC, Korea).

Conflict of interest statement: The authors declare no conflict of interest.

Data availability statement: Data openly available in a public repository that issues datasets with DOIs.

Received: *18 July 2023* Accepted: *7 November 2023*
doi: 10.1049/ell2.13026

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