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Wafer-scale integration of transition metal dichalcogenide field-effect transistors using adhesion lithography

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Field-effect transistors based on two-dimensional materials are a potential replacement for silicon-based devices in next-generation semiconductor chips. However, the weak interfacial adhesion energy between two-dimensional materials and substrates can lead to low yields and non-uniform transistors on the wafer scale. Furthermore, conventional photolithography processes—including photochemical reactions and chemical etching—can damage atomically thin materials. Here we show that the interfacial adhesion energy between two-dimensional materials and different substrates can be quantified using a four-point bending method. We find that a molybdenum disulfide/silicon dioxide interface has an interfacial adhesion energy of 0.2 J m^{-2}, which can be modulated from 0 to 1.0 J m^{-2} by incorporating self-assembled monolayers with different end-termination chemistries. We use this to create an adhesion lithography method that is based on adhesion energy differences and physical etching processes. We use this approach to fabricate more than 10,000 molybdenum disulfide field-effect transistors on six-inch wafers with a yield of around 100%.

Transition metal dichalcogenides (TMDs) are a potential replacement for silicon in field-effect transistors (FETs) because of their atomically thin structure that has no dangling bonds and a bandgap that is similar to that of silicon[1]. However, despite progress in terms of fundamental materials and device development, reliable device integration across an entire wafer remains challenging[1,2]. The interfacial properties between two-dimensional (2D) materials and different substrates—including metals, insulators and other 2D materials—are crucial in determining the performance and reliability of 2D FETs[3,4]. Furthermore, the weak interfacial adhesion energy (IAE) between 2D materials and substrates can lead to low yields and non-uniform 2D FETs on the wafer scale[5–7]. Furthermore, conventional photolithography processes, such as photochemical reactions and chemical etching, are often too aggressive and can damage atomically thin materials, leading to reproducibility issues and a lack of uniformity[8].

To improve such devices, it is essential to quantify the IAE values of various large-scale interfaces and their consistency. Numerous attempts have been made to theoretically and experimentally quantify the IAE values of systems with 2D materials[9–12]. However, the reported IAE values vary considerably[12,13]. Moreover, the measurement setup and sample preparation of most existing methods are relatively complex

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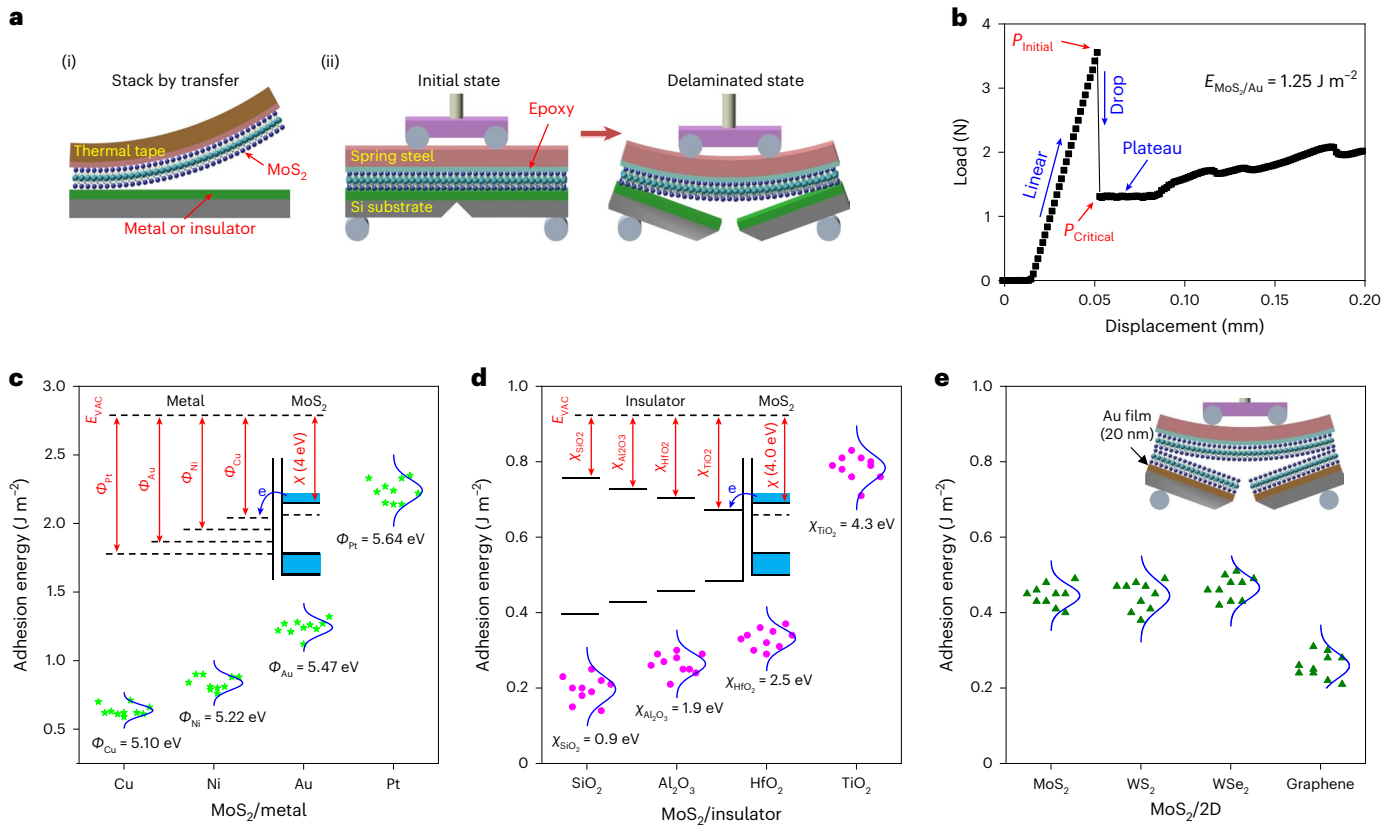

Fig. 1 | Quantification of the IAE value of MoS_2/metal, MoS_2/insulator and MoS_2/2D using a four-point bending method. a, Schematic of MoS_2 transfer (i) and the four-point bending method at the initial and delaminated states (ii). **b**, Typical load–displacement curve from the four-point bending measurement. **c**–**e**, Measured IAE of the MoS_2/metal (**c**), MoS_2/insulator (**d**) and MoS_2/2D interfaces (**e**). Here, Φ is the work function of the metal, χ is the electron affinity of MoS_2 or insulator and E_{VAC} is the reference vacuum level. The insets in **c** and **d** are the band diagrams of metal/MoS_2 and insulator/MoS_2, respectively. The inset in **e** is a schematic of the IAE measurement setup used for the MoS_2/MoS_2 films supported by a Au film (20 nm).

and unsuitable for the analysis of large-scale interface analysis required for industrial applications.

In this Article, we show that the IAE values between 2D materials and different substrates can be quantified using a four-point bending method (Fig. 1a)[14]. We use 2D materials—including molybdenum disulfide (MoS_2) and graphene—grown by chemical vapour deposition (CVD), which allows us to study the effect of intrinsic defects on the IAE value over a large area. Interfaces are formed by transferring the CVD material onto a metal or insulating layer, an approach that limits the creation of artefacts during the stacking process (Fig. 1a(i)). A MoS_2/silicon dioxide (SiO_2) interface is found to have an IAE value of only 0.2 J m^{-2}. This interface is then modified using self-assembled monolayers (SAMs) with different end terminations—fluoro (CF_3–), methyl (CH_3–), thiol (–SH) and amine (NH_2–)—which modulates the IAE value from around 0 to 1 J m^{-2}. Based on the differences in IAE between MoS_2/CF_3–SAM (~0 J m^{-2}) and MoS_2/SH–SAM (~0.5 J m^{-2}) interfaces, we develop an adhesion lithography process for patterning MoS_2. We use this approach to fabricate more than 10,000 MoS_2 FETs on six-inch wafers with a yield of around 100%.

IAE between MoS_2 and substrates

The detailed sampling processes and measurement setup are shown in Supplementary Figs. 1 and 2. The substrates of the samples were notched to form a pre-crack (Fig. 1a(ii)). The IAE values of MoS_2/metal and MoS_2/insulator systems were systematically quantified using the four-point bending method. The displacement rate was kept constant (0.4 μm s^{-1}) for the entire measurement. At the initial state, when the displacement is constantly increased, the load increases linearly. The displacement increases until the fracture strength of the Si substrate is reached at an initial load ($P_{Initial}$), and a crack begins to form along the weakest interface. The crack then propagates along the weakest interface (MoS_2/substrate interface; Fig. 1a,b) at a critical load ($P_{Critical}$) because the centre of the specimen is under a constant moment (observed as a plateau in the curve). A sharp drop in the measured load indicates the delaminated state. The IAE value is calculated from $P_{Critical}$ (Supplementary Equation (1)) and was found to be 1.25 J m^{-2} for the MoS_2/gold (Au) interface.

The IAE value between the two materials is mainly due to covalent bonding, electrostatic force and van der Waals forces. The covalent bonding is formed when atoms of the two materials share or exchange electrons. The electrostatic forces originate from charge transfer due to the difference in surface potential between the two materials. The van der Waals forces are caused by physisorption between the two materials. The IAE value between MoS_2 and metal is strongly correlated with the work function of the metal (Fig. 1c). The IAE value between MoS_2 and copper (Cu), nickel (Ni), Au and platinum (Pt) was observed to be $E_{MoS2/Cu}$ (0.64 ± 0.03 J m^{-2}), $E_{MoS2/Ni}$ (0.84 ± 0.04 J m^{-2}), $E_{MoS2/Au}$ (1.25 ± 0.05 J m^{-2}) and $E_{MoS2/Pt}$ (2.24 ± 0.06 J m^{-2}), respectively, and followed the same increasing trend as the respective work functions (Φ) of the metals (Φ_{Cu} (5.10 eV), Φ_{Ni} (5.22 eV), Φ_{Au} (5.47 eV) and Φ_{Pt} (5.64 eV)).

The IAE value of the MoS_2/metal interface mainly arises from the charge-transfer-induced electrostatic forces. The Φ values of all the metals used here are higher than the electron affinity of MoS_2 (~4 eV)[15]. Hence, the electrons tend to transfer from MoS_2 to the metal to achieve a constant Fermi level at the interface (Fig. 1c, inset). Fermi-level pinning did not occur as the MoS_2 film was transferred to the metal surface[3,16].

This charge transfer probably induces a depletion region with positive ions in MoS_2 and negative ions in the metal, causing an electrostatic force at the MoS_2/metal interface. A higher number of transferred charges induces a higher electrostatic force, resulting in higher IAE. This was confirmed using X-ray photoelectron spectroscopy (XPS), which shows that the amount of charge transfer was directly proportional to the difference between Φ of the metal and electron affinity of MoS_2 (Supplementary Fig. 3). Covalent bonding between the metal and sulfur atoms could also contribute to the IAE value[17–19]. However, metal–sulfur bonds were not observed in the XPS measurements (Supplementary Fig. 3b). The native oxide on the metal surface (Cu or Ni) reduces the IAE value (Supplementary Fig. 4). Hence, we concluded that the contribution of covalent bonding to IAE was negligible.

Figure 1d shows the IAE values between MoS_2 and insulators with different dielectric constants. In general, the dielectric constant and electron affinity of an insulator are proportional[20]. Similar to those of the MoS_2/metal interfaces, the IAE values of the MoS_2/insulator interfaces were mainly induced by the electrostatic forces and were well correlated with the electron affinity of the insulator. The IAE values increased in the following order for silicon dioxide (SiO_2), aluminium oxide (Al_2O_3), hafnium oxide (HfO_2) and titanium dioxide (TiO_2): $E_{MoS2/SiO2}$ (0.20 ± 0.03 J m^{-2}) < $E_{MoS2/Al2O3}$ (0.26 ± 0.02 J m^{-2}) < $E_{MoS2/HfO2}$ (0.33 ± 0.02 J m^{-2}) < $E_{MoS2/TiO2}$ (0.78 ± 0.03 J m^{-2}). Insulators with a higher electron affinity had stronger adhesion with MoS_2 (Fig. 1d (inset) and Supplementary Fig. 5). The effect of the substrate's surface roughness on the difference in the IAE value was considered to be negligible as the average roughness between the metals and between the insulators was measured to be similar (Supplementary Fig. 6). The delamination along the MoS_2/metal or MoS_2/insulator interface during the four-point bending test was confirmed (Supplementary Fig. 7).

The IAE value between MoS_2 and other 2D materials (tungsten disulphide (WS_2), tungsten diselenide (WSe_2) and graphene) is shown in Fig. 1e. Supplementary Fig. 8 shows a representative example of MoS_2/MoS_2 stacked on a Au support film. Here, Au was chosen as it is an inert substrate and has a relatively high IAE value with MoS_2 (Fig. 1c). Hence, delamination occurred along the weakest interface, namely, the MoS_2/MoS_2 interface, as $E_{Au/MoS2(bottom)} > E_{MoS2(top)/MoS2(bottom)}$ (Fig. 1c–e). Using the Au support film, we could quantify the IAE values for various 2D/2D interfaces. The delamination always occurred along the 2D/2D interface (Supplementary Fig. 9). The IAE values of stacked MoS_2/MoS_2, MoS_2/WS_2 and MoS_2/WSe_2 films were found to be similar and ranged from 0.45 to 0.47 ± 0.03 J m^{-2}. The charge transfer between the TMD materials with similar electron affinity is negligible, indicating that the dominant contribution to the IAE value at the MoS_2/MoS_2 interface was the van der Waals interactions. The IAE value of the MoS_2/MoS_2 interface was observed to increase with thermal annealing. The value saturated after 100 min due to the removal of water and/or air gaps at the interface[21]. The saturated IAE value was found to be similar to that of as-grown MoS_2/MoS_2 (Supplementary Fig. 10). The IAE value of MoS_2 and graphene was measured to be lower than that of MoS_2 and other TMD interfaces, which is consistent with the inertness of graphene and the larger lattice mismatch between MoS_2 and graphene compared with other TMD systems. The IAE value of MoS_2/graphene was observed to be inversely proportional with the graphene grain size (Supplementary Fig. 11).

IAE modulation of MoS_2/insulator by SAMs

Insulators like SiO_2, Al_2O_3 and HfO_2 have been widely used as a gate dielectric in 2D FETs. However, MoS_2 films weakly adhere to insulators, leading to a low yield and device uniformity because the MoS_2 film can be easily peeled off during device fabrication[1,2,6]. This weak adhesion can be visualized by the detachment of MoS_2 from its substrate in water[5] and was further quantified by our measurements (Fig. 1d). Therefore, improving the adhesion of MoS_2 with insulators is needed for reliable integration. SAMs have been widely used to study the interface characteristics in various applications[22–25]. To control the IAE value of a TMD material/insulator interface using SAMs with various end-termination chemistries (namely, CF_3–, CH_3–, –SH and NH_2–), we chose to functionalize the SiO_2 interface as it initially showed the weakest adhesion energy at the interface, and we systematically studied the SAM's influence on the MoS_2/insulator IAE values. SAM layers with various terminal groups were uniformly grown on six-inch SiO_2 wafers, as evidenced by the water contact angle (WCA), atomic force microscopy (AFM) and spectroscopic ellipsometry mapping results (Supplementary Figs. 12 and 13).

Figure 2a shows the simplified ball-and-stick models of the four SAMs used here and an illustration of MoS_2 on an SH-treated SiO_2 substrate. The IAE values between MoS_2 and various SAM-treated SiO_2 substrates were well correlated with the electron ability of the SAM end group (Fig. 2b). The IAE values increased with electron abundance: $E_{MoS2/CH3\text{-}SiO2}$ (0.12 ± 0.03 J m^{-2}) < $E_{MoS2/Bare\text{-}SiO2}$ (0.20 ± 0.03 J m^{-2}) < $E_{MoS2/SH\text{-}SiO2}$ (0.49 ± 0.02 J m^{-2}) < $E_{MoS2/NH2\text{-}SiO2}$ (0.98 ± 0.03 J m^{-2}). The XPS measurements were performed to reveal the charge transfer and binding structure of MoS_2 on various SAM-treated SiO_2 substrates (Fig. 2c–e). Relative to those of MoS_2/bare SiO_2, the Mo3*d* peaks were downshifted by 0.21 eV to a lower binding energy for MoS_2/NH_2–SiO_2, suggesting that the MoS_2 film was p doped. This p doping mainly occurs due to the charge transfer as a result of nitrogen atoms filling the sulfur vacancies in the MoS_2 lattice and forming N–Mo covalent bonds, as demonstrated by theoretical and experimental results[26,27]. The formation of N–Mo covalent bonds via S vacancies was further proved here (Fig. 2d and Supplementary Figs. 14 and 15). In contrast, an upshift of 0.36 eV in the Mo3*d* peaks was observed for MoS_2/SH–SiO_2, indicating that the MoS_2 film was n doped, where S vacancies in MoS_2 were filled by S atoms from the SH (Fig. 2e and Supplementary Fig. 16)[28]. No shift in the Mo3*d* peaks was observed for MoS_2/CH_3–SiO_2, suggesting that MoS_2 did not interact with CH_3–SAM. We further investigated the interactions between MoS_2 and four kinds of SAM-treated SiO_2 substrates using photoluminescence (PL) measurements (Fig. 2f), where the measurement conditions (such as laser intensity and acquisition time) for all the samples were kept identical (Methods). Specifically, we observed the PL-quenching phenomena for MoS_2/NH_2–SiO_2. During the PL measurement, nitrogen from the NH_2 groups is thermodynamically favourable for trapping the excited electrons owing to its relatively high electronegativity (3.04) (ref. 29), resulting in PL quenching; this confirms the incorporation of nitrogen in the MoS_2 lattice. In contrast, PL enhancement was observed for MoS_2/SH–SiO_2. This was attributed to S vacancies being filled by S from the SH groups, consistent with the XPS data. No peak shift or intensity change was observed for MoS_2/CH_3–SiO_2, again indicating that MoS_2 did not react with the CH_3 groups. Because of the formation of covalent bonds (N–Mo and S–Mo), the IAE values of MoS_2/NH_2–SiO_2 and MoS_2/SH–SiO_2 were higher than those of MoS_2/SiO_2 and MoS_2/CH_3–SiO_2. The higher IAE value of MoS_2/NH_2–SiO_2 than MoS_2/SH–SiO_2 was because N–Mo bonds are stronger than S–Mo bonds[26,27]. The adhesion between MoS_2 and SAM-treated SiO_2 substrates was visualized by sonication tests (Fig. 2g). Immediately after transfer, uniform MoS_2 films were observed on bare SiO_2, NH_2–SiO_2 and SH–SiO_2 substrates. The MoS_2 film partially peeled off from the CH_3–SiO_2 substrate due to weak interfacial adhesion. After sonication in acetone, much of the MoS_2 film was removed from the bare SiO_2, and almost all the MoS_2 immediately detached from the CH_3–SiO_2 substrate on immersion in acetone. In contrast, the MoS_2 film on the NH_2–SiO_2 and SH–SiO_2 substrates remained unchanged after 3 min of sonication due to strong adhesion. No data are available for MoS_2 on CF_3–SiO_2 because MoS_2 could not be successfully transferred onto this substrate, which suggests that MoS_2 adhered very weakly to CF_3–SiO_2 ($E \approx 0$ J m^{-2}). The IAE value between graphene and SiO_2 substrate treated with a range of SAMs was influenced by the charge transfer determined by the electron ability of the SAM (Supplementary Fig. 17).

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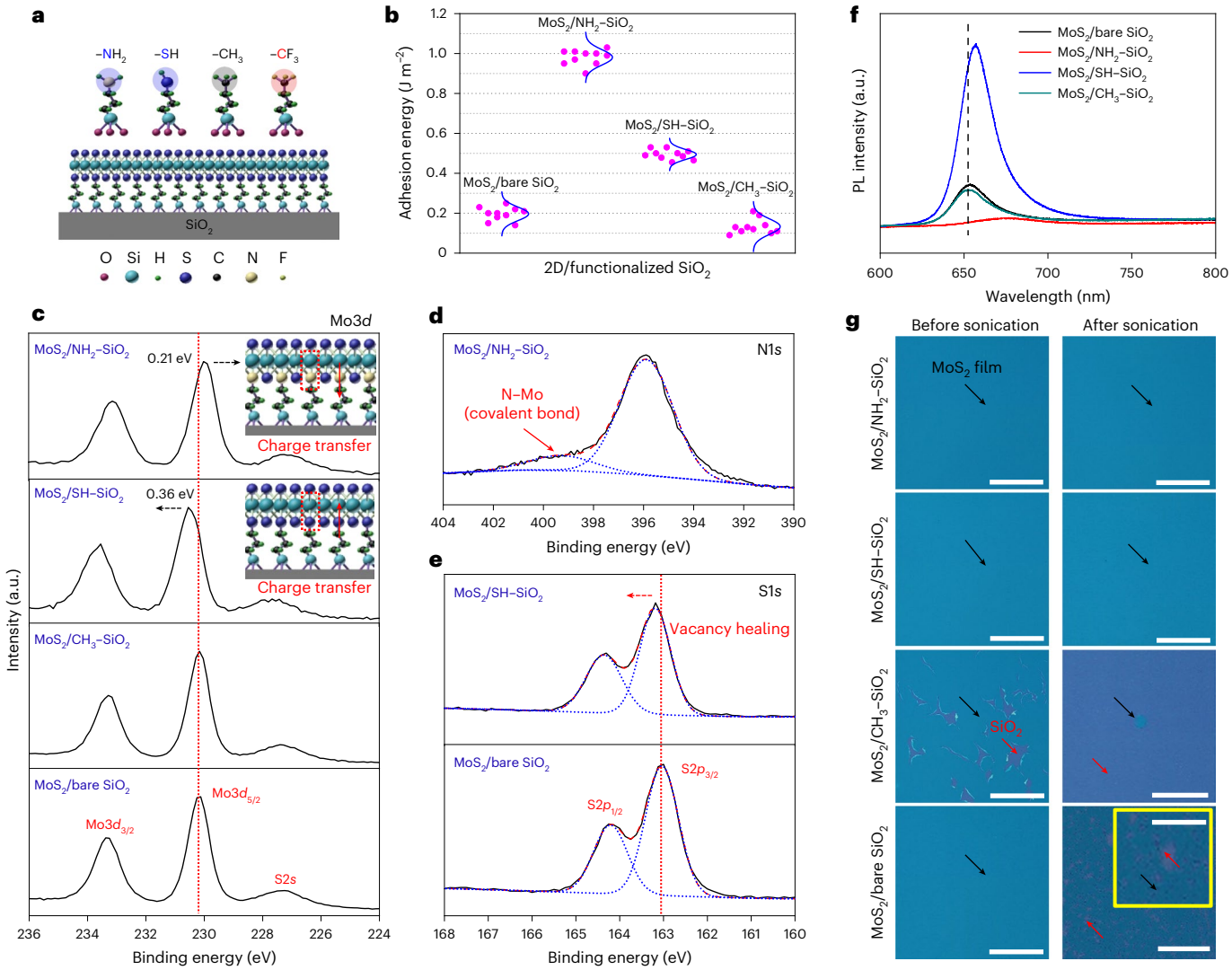

Fig. 2 | Engineering the adhesion energy of MoS_2/insulator interface with various SAMs. a, Simplified ball-and-stick models of the four kinds of SAMs used in surface functionalization and an example illustration of MoS_2 on the SH–SAM-treated SiO_2 substrate. **b**, Measured IAE value between MoS_2 and various SAM-treated SiO_2 substrates. Statistical analysis yields IAE values between MoS_2 and CH_3–SiO_2, bare SiO_2, SH–SiO_2 and NH_2–SiO_2 as 0.12 ± 0.03, 0.20 ± 0.03, 0.49 ± 0.02 and 0.98 ± 0.03 J m^{-2}, respectively. These values represent the mean ± standard deviation. The statistics in each case are obtained from ten independent IAE measurements. **c**–**e**, XPS spectra of Mo3*d*, N1*s* and S1*s* of MoS_2 on different SAM-treated SiO_2 substrates. The dotted rectangle and arrows in **c** depict the Mo–N and Mo–S bonding and charge transfer direction, respectively. **f**, PL spectra of MoS_2 on the various SAM-treated SiO_2 substrates. **g**, Optical microscopy images of MoS_2 on different SAM-treated SiO_2 substrates before (left) and after (right) sonication in acetone for 3 min. Scale bars, 100 µm. The insets show the enlarged optical images. Scale bars, 50 µm. The black and red arrows depict the MoS_2 film and SiO_2, respectively.

Adhesion lithography

The most common method of patterning TMD materials is a top-down approach, where photolithography or electron-beam lithography is used to define the channel and reactive ion etching is subsequently used to etch the unwanted areas. However, this approach requires toxic etching gases[30] and can induce residues due to polymer hardening, which occurs during etching under a plasma environment. By controlling the IAE value between TMD materials and substrate via interface chemistry, we provide a method for patterning TMD films that does not require photolithography and reactive ion etching processes and can ensure that the patterned TMD films reliably adhered to the substrate.

Figure 3a illustrates the adhesion lithography method in three primary steps. In step one, a two-component SAM film with alternating stripes of SH–SAM and CF_3–SAM was prepared. An SH–SAM layer was then deposited over the entire substrate and then patterned using ultraviolet light through a non-contact photomask (Supplementary Fig. 18). The exposed areas of the SH–SAM layer were decomposed by the ultraviolet light, followed by the selective growth of CF_3–SAM on the irradiated area, to form a coplanar SAM film (SH–SAM/CF_3–SAM) (ref. 31). Figure 3b clearly indicates that coplanar CF_3–SAM/SH–SAM was successfully prepared. The WCA value of the photoirradiated area was measured to be <5° and 98° before and after CF_3–SAM treatment, respectively, whereas the WCA value of the SH–SAM area remained unchanged (72–74°) (Supplementary Fig. 19). In step two, a MoS_2 film was transferred onto the coplanar SAM film, followed by sonication in acetone in step three. MoS_2 on the CF_3–SAM area with nearly zero IAE was easily detached, leaving MoS_2 patterned on the SH–SAM area due to the higher IAE of ~0.5 J m^{-2}.

We refer to this method as adhesion lithography since it is based on the adhesion energy difference and physical etching process. Although SH–SAM would easily decompose under ultraviolet irradiation, its

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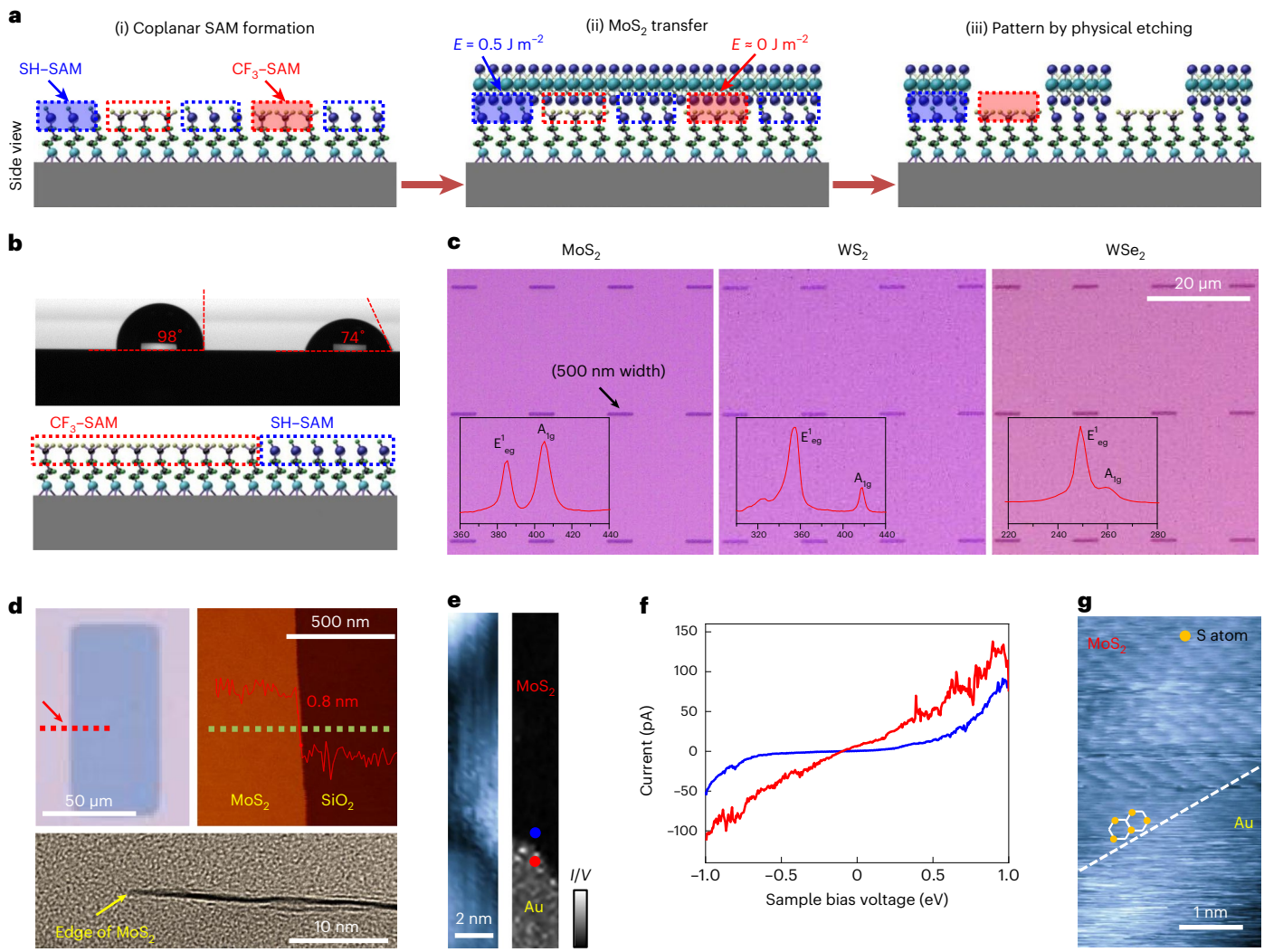

Fig. 3 | Patterning method for MoS_2 without photolithography and etching processes. a, Side-view schematic of the MoS_2 patterning processes. Pre-patterning of the coplanar SH–SAM/CF_3–SAM-treated substrate (i). Transfer of the MoS_2 film to the coplanar SAM-treated substrate (ii). MoS_2 film was physically patterned by sonication in acetone (iii). MoS_2 remained only on the SH–SAM-treated region and was removed from the CF_3–SAM-treated region. **b**, Schematic and corresponding WCA value of coplanar CF_3–SAM/SH–SAM surfaces. **c**, Optical microscopy images of a patterned MoS_2, WS_2 and WSe_2 sample. The inset shows the corresponding Raman spectra. **d**, Optical microscopy image and AFM image of MoS_2 pattern (top) and high-resolution cross-sectional transmission electron microscopy image at the edge of the MoS_2 pattern (bottom). The red-dotted line in the optical microscopy image shows the focused-ion-beam position that cuts across the edge of MoS_2. **e**, STM image at the junction between MoS_2/Au and Au (left) and the corresponding *I*–*V* map (right). **f**, *I*–*V* spectra taken at the position indicated by the blue and red dots in **e**. **g**, Close-up STM image at the boundary between MoS_2/Au and Au.

stability in air and water for up to 4 days was confirmed (Supplementary Fig. 20). Optical microscopy images for each step in the process are shown in Supplementary Fig. 21. Adhesion lithography can be applied to various TMD materials. Optical microscopy imaging, Raman and PL data are three examples of patterned arrays of MoS_2, WS_2 and WSe_2 with a minimum spatial resolution down to 500 nm (Fig. 3c and Supplementary Fig. 22). This method is more environmentally friendly, as it does not use a photoresist and toxic gases in the etching processes. Moreover, it can remarkably reduce the formation of artefacts such as defects, tears and residues compared with the conventional etching process, so that the intrinsic properties of the TMD materials can be maintained even after patterning.

Both top-view (optical microscopy (top left) and AFM (top right) images; Fig. 3d) and side-view (cross-sectional transmission electron microscopy; Fig. 3d (bottom)) at the edge region of the MoS_2 pattern shows that MoS_2 was patterned with clean edges. On the other hand, the MoS_2 pattern fabricated by conventional photolithography shows that MoS_2 at the edge was folded to form a multilayer edge (Supplementary Fig. 23). This was caused by the weak IAE of the MoS_2/substrate interface and a folding of MoS_2 as the photoresist was chemically removed. Scanning tunnelling microscopy (STM) measurement was performed to observe the edge structure of MoS_2 at an atomic resolution. The STM sample preparation method is provided in the Methods section. Figure 3e displays the STM image (left) and corresponding current–voltage (*I*–*V*) mapping (right) at the junction between MoS_2/Au and Au. The distinct contrast shown in the *I*–*V* mapping, as well as the corresponding *I*–*V* curve shown in Fig. 3f, confirms a clear boundary between MoS_2/Au and Au. The high-resolution image of the boundary between MoS_2/Au and Au indicated that the edge of the patterned MoS_2 has a zigzag structure (Fig. 3g).

The peeling off or lifting of TMD materials induced by fabrication processes is more serious than that induced by manual laboratory processes. This is because the standard fabrication processes typically employ harsh chemical and sonication during development and

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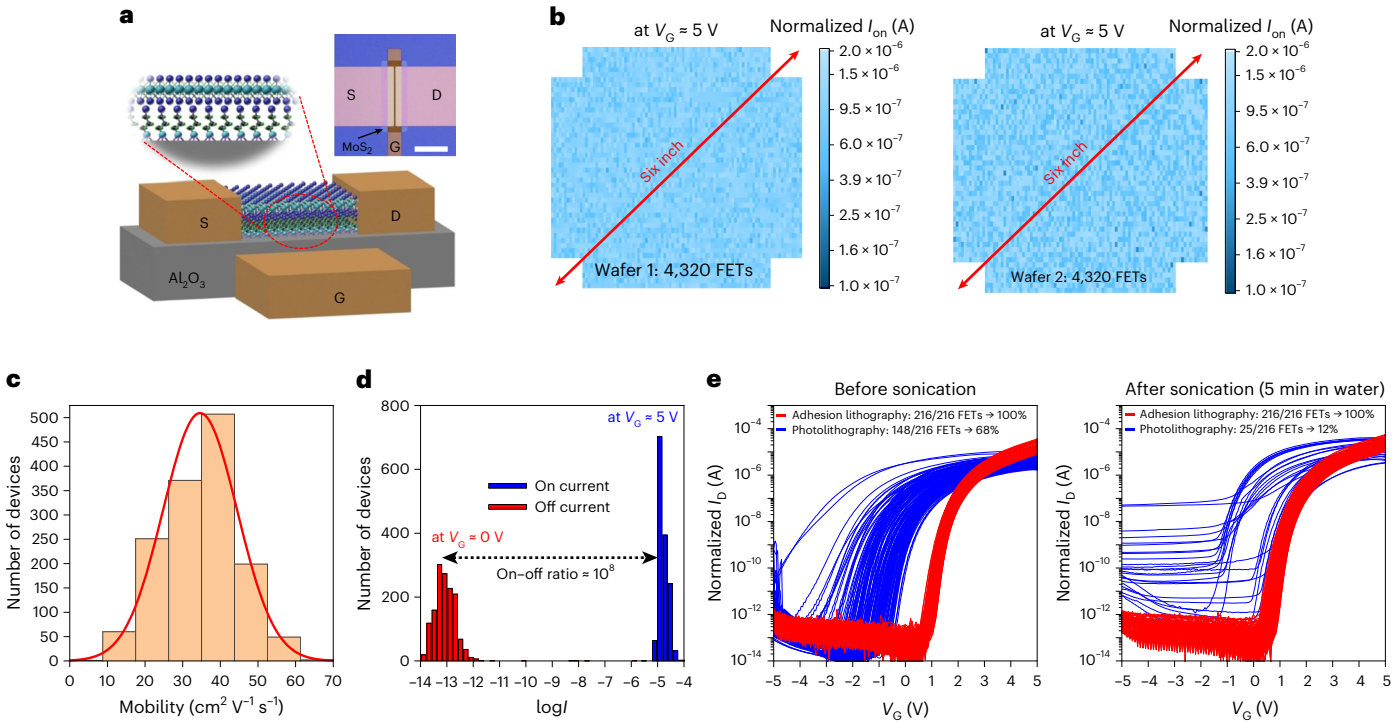

Fig. 4 | FET uniformity over a six-inch wafer. a, Schematic of a local back-gate FET with a MoS_2 channel on an SH–SAM-treated substrate. The inset shows the optical microscopy image of a typical FET (scale bar, 50 µm). S, source; D, drain; G, gate. **b**, Two colour maps (collected from 8,640 devices) of the normalized on current. Each coloured pixel corresponds to an individual device. The FETs were fabricated using a six-inch MoS_2 film with a grain size of 40 nm. **c**,**d**, Histogram of the mobility values (**c**) and on–off current (log scale) (**d**) from 1,440 FETs, which were fabricated using 5 × 10 cm^2 MoS_2 film with a grain size of 500 nm. **e**, Typical I_D–V_G curves from three representative dies before and after the sonication of FETs, which were fabricated by adhesion lithography (red) and conventional photolithography (blue).

lift-off processes, which are necessary for clean fabrication in an industrial setting. Therefore, improving the IAE value of the TMD/substrate is ultimately important for fundamental studies and also for reliable device integration using fabrication processes. In this work, we realized the batch fabrication of homogeneous and high-yield FETs on six-inch Si wafers (Fig. 4) using adhesion lithography and industry-standard fabrication processes. The FET fabrication process is described in the Methods section. An individual local back-gate FET consisting of a MoS_2 channel on an SH–SAM-treated Al_2O_3 substrate is shown in Fig. 4a (the inset shows an optical microscopy image of a typical device). A total of 4,320 FETs were fabricated over the entire six-inch wafer using 40-nm-grain-size MoS_2 (Supplementary Fig. 24). The I–V characteristics of all the FETs were measured using an automated probe station to obtain the statistics on the quality of devices. Figure 4b shows two colour maps of the normalized on current ($I_{Normalized} = I\frac{L}{W}$, where W and L are the channel width and length, respectively) of all the devices across the entire six-inch wafer; each coloured pixel corresponds to an individual device. The yield across both wafers was close to 100% (8,640 FETs) with small device-to-device variations in the on current at $V_G \approx 5$ V. This shows the excellent uniformity across each wafer and wafer-to-wafer uniformity for devices fabricated from IAE-controlled MoS_2/SH–SiO_2. The uniform conductance switching behaviour with high on–off ratio (5×10^7) and mobility values of FETs were calculated with an average value of 4.8 $cm^2\,V^{-1}\,s^{-1}$ and a standard deviation of 0.8 $cm^2\,V^{-1}\,s^{-1}$ (Supplementary Fig. 25a–d). Using a MoS_2 film with a large grain size of ~500 nm (ref. 32), an FET device fabricated by adhesion lithography with high uniformity and high yield (100%) was realized. The mobility values of 1,440 FETs across 5 × 10 cm^2 were calculated, with an average value of 35 $cm^2\,V^{-1}\,s^{-1}$ and maximum at 70 $cm^2\,V^{-1}\,s^{-1}$ (Fig. 4c and Supplementary Fig. 26a). The tight distribution of mobility indicated the electrical homogeneity of the devices. The histogram of the on state at $V_G \approx 5$ V and off state at $V_G \approx -5$ V had a strong peak near 2×10^{-5} (A) and 8×10^{-14} (A), respectively (Fig. 4d), indicating a uniform conductance switching behaviour with a high on–off ratio (~10^8). We emphasize that although uniformity has been shown in previous works, the statistical measurements were limited to a specific region within 200 FETs (refs. 32,33). Here, we have demonstrated excellent uniformity and yield by analysing more than 10,000 FETs across the entire six-inch wafer, approaching the industry standard.

In contrast, MoS_2 FET devices fabricated by conventional photolithography on bare Al_2O_3 substrates exhibited non-uniform I_D–V_G curves, lower yield of 70% and large variations in the on current (Supplementary Figs. 25e–h and 26b). The higher device performance (mobility, on–off ratio) of FETs fabricated by adhesion lithography was attributed to the well-defined pattern (Supplementary Fig. 24c), lower contact resistance (Supplementary Fig. 27) and S vacancy healing by SH–SAM (Supplementary Fig. 28)[24]. The uniformity of p-type materials such as a WSe_2 FET produced using our patterning method was also confirmed (Supplementary Fig. 29), indicating the applicability of our patterning method to both p- and n-type materials. Our patterning method offers the advantage of processing stability due to the high IAE value between MoS_2 and SH–SAM-treated substrate, especially under harsh conditions. We found that 100% of the FETs fabricated by adhesion lithography survived 5 min of water sonication, whereas the I_D–V_G transfer curves barely changed (Fig. 4e, red curves). On the other hand, only 12% of the FETs fabricated by conventional photolithography survived and the I_D–V_G transfer curves mostly degraded after being subjected to the same amount of sonication (Fig. 4e, blue curves).

Conclusions

We have shown that the IAE characteristics of various types of interface can be systematically quantified and understood using four-point bending methods. The IAE values of systems containing TMD materials were modified using SAMs with different end-termination chemistries; this approach can be used to increase the IAE value by a factor of two to five times. By exploiting these differences in IAE, a patterning method for MoS_2 was developed and used to fabricate 2D FETs with high yield, spatial uniformity and reproducibility. Our work suggests that understanding and engineering IAEs can provide a route to transition 2D devices from laboratory to industrial fabrication with reliable integration.

Methods

Four-point bending specimen preparation

A 20-nm-thick metal or insulator film was prepared on a six-inch Si substrate (thickness, 700 μm), followed by MoS_2 transfer by a conventional polymethyl methacrylate-assisted method[5]. Tape was attached to the MoS_2 film to protect it during dicing into several tens of specimens with dimensions of 6.0 mm × 60.0 mm (with a pre-crack depth of 0.4 mm), and the tape was then removed. The specimens were bonded to spring steels using epoxy (EpoTek 353ND consisting of bisphenol F and imidazole; Epoxy Technology). The specimens were press cured in a dry oven at 90 °C for 2 h to guarantee strong adhesion between the spring steel and MoS_2 film. Detailed procedures are presented in Supplementary Fig. 1. The load–displacement curves were measured using a microload system (R&B).

SAM treatment

All the chemicals used in the SAM treatment were purchased from Sigma-Aldrich. Before the SAM treatment, an oxide wafer was treated by oxygen plasma (2,500 W, 1,000 mtorr, 90 s, 180 °C, 2,500 s.c.c.m. O_2 and 250 s.c.c.m. N_2) to remove organic residues and form a hydroxyl-terminated oxide surface. In the case of (3-aminopropyl)triethoxysilane (NH_2–SAM), the plasma-treated wafer was immersed in a 1% (v/v) NH_2–SAM/ethanol solution for 1 h. Other SAMs, such as (3-mercaptopropyl)trimethoxysilane (SH–SAM), *n*-propyltriethoxysilane (CH_3–SAM) and (3,3,3-trifluoropropyl)trimethoxysilane (CF_3–SAM), were prepared by CVD as follows. First, 0.5 ml of the SAM precursor was dropped into a Teflon container. The plasma-treated wafer was placed inside this container 5 cm away from the source. The container was sealed with a cap and then heated to 150 °C over 3 h and then naturally cooled down to room temperature.

TMD synthesis

Cold-wall metal–organic CVD was used to grow MoS_2, WS_2 and WSe_2 films on six-inch Si wafers with a 100 nm SiO_2 surface layer. $Mo(CO)_6$, $W(CO)_6$, $(C_2H_5)_2S_2$ and $(C_2H_5)_2Se_2$ were selected as the precursors of Mo, W, S and Se, respectively. The precursors were diluted in a N_2 carrier gas and precisely injected into the chamber by mass flow controllers and electronic pressure controllers. The flow rates of the precursors were 0.024 s.c.c.m. for $Mo(CO)_6$ or $W(CO)_6$, 0.990 s.c.c.m. for $(C_2H_5)_2S_2$ or $(C_2H_5)_2Se_2$ and 100.000 s.c.c.m. for H_2. After 2 min of injection, the precursor flow was stopped, and the system was purged by N_2 gas for 1 min, resulting in a total growth time of 3 min for each cycle. Full coverage of a monolayer of TMD was obtained after four growth cycles. The temperature and total pressure were 900 °C and 5.0 torr, respectively, during the growth process[34]. MoS_2 with a grain size of 500 nm was grown using the NaCl-assisted method[32].

Device fabrication and measurement

The entire fabrication process was done using fabrication-standard processes, including the chemicals (stripper and developer). The bottom gate electrode was defined using a standard photolithography process, followed by electron-beam evaporation of Ti(1 nm)/Au(20 nm). Then, a 20 nm Al_2O_3 film was deposited as a gate dielectric using atomic layer deposition. A MoS_2 channel was patterned by our developed method (Fig. 3). Then, a 30 nm Au film was deposited by electron-beam evaporation for defining the source/drain contact. Finally, a 20 nm Al_2O_3 film was deposited by atomic layer deposition for passivation. The *I*–*V* characteristics of the fabricated FET devices were measured using a Keithley 4200A SCS (Tektronix) semiconductor parameter analyser with an automated probe station.

STM/scanning tunnelling spectroscopy measurements

We performed the experiments with a commercial low-temperature STM instrument (RHK) at 4.2 K in an ultrahigh vacuum (pressure, $<1.0 \times 10^{-10}$ torr). The sample was prepared as follows. A 50 nm Au film was deposited on pre-patterned MoS_2 on a SAM-treated SiO_2/Si wafer, after which an STM plate was attached to the Au surface using conductive epoxy. Then, the STM plate/Au/patterned MoS_2 was detached from SiO_2/Si in a high-vacuum chamber ($<10^{-7}$ torr) at room temperature to prevent contamination of the MoS_2 surface. The sample was then moved to the low-temperature STM chamber, in which the temperature was maintained at 4.2 K. To clarify the edge of the MoS_2 pattern on Au, we performed scanning tunnelling spectroscopy using a conventional lock-in technique with a modulation voltage of 10 mV at a frequency of 1 kHz.

PL measurements

The measurement was carried out using Renishaw equipment in the ambient environment. All the measurements in this study were performed in the same condition with 10 s exposure time and 100% laser power.

Data availability

Data that support the findings of this study are available from the corresponding author upon reasonable request.

Code availability

The computer code used in this study is available from the corresponding author upon reasonable request.

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Author contributions

V.L.N. conceived the main idea, performed most of the experiments and interpreted the data. M.S. synthesized MoS_2 and WS_2 and interpreted the experimental data. J.K. wrote the program for the extraction of FET properties. E.-K.L. contributed to the four-point bending machine setup. W.-J.J. and H.W.K. performed the STM measurement. C.L., J.H.K. and J.P. provided the 500-nm-grain-size MoS_2 and WSe_2. M.S.Y. performed the WSe_2 growth. V.L.N. and H.-J.S. wrote the manuscript. H.-J.S. supervised this project. All the authors discussed the results and commented on the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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