ADVANCED FUNCTIONAL MATERIALS
www.afm-journal.de

A Van der Waals Optoelectronic Synapse with Tunable Positive and Negative Post-Synaptic Current for Highly Accurate Spiking Neural Networks

Hyejin Yoon, Soeun Park, Yeong Kwon Kim, Juhwan Baek, Ki Han Kim, Seongil Yun, Hyeonchang Son, Jeongeun Choi, Byung Chul Jang, and Dong-Ho Kang**

Spiking neural networks (SNNs) represent a promising computing architecture for neuromorphic hardware, as they process and store information through spike signals, closely mimicking the way the human brain operates. However, most synaptic devices recently proposed for hardware SNN implementations are limited to exhibiting analogue tuning within a single conductance polarity, making them inadequate for realizing scalable and energy-efficient neuromorphic systems. In this study, an optoelectronic synaptic device based on a ReS_2/WSe_2/*h*-BN heterostructure, enabling conductance modulation across both positive and negative states within a single device is demonstrated. This bidirectional plasticity originates from electrostatic modulation of the WSe_2 Fermi level, induced by voltage pulses applied through an O_2 plasma-treated *h*-BN weight-control layer. The device exhibits reversible photocurrent polarity, reliable potentiation/depression of the postsynaptic current, and stable synaptic weight retention with reproducible multi-cycle operation. System-level simulations using a 1024–20–3 SNN architecture confirmed the functional advantage of a bidirectional synapse, with networks achieving over 95% facial recognition accuracy within 20 training epochs, whereas the unidirectional synapse-based network plateaued below 75%. These findings highlight the potential of optoelectronic synaptic device with bidirectional plasticity as a promising device platform for efficient on-chip learning in next-generation neuromorphic hardware system.

1. Introduction

As the use of Artificial Intelligence (AI)-based hardware devices has increased exponentially, the von Neumann computing architecture has reached its limits in transmitting exponentially increasing amounts of data due to von Neumann bottleneck caused by the separation of memory and computation regions.[1] To overcome this fundamental throughput limitation, researchers have been exploring next-generation computing architectures that have the ability to conduct data processing and memorization in a parallel manner.[2–5] Recently, neuromorphic computing based on artificial neural networks (ANNs) has emerged as a promising solution to these problems. This computing architecture mimics the parallel and event-driven processing of the human brain.[6,7] Among the various neural network models proposed thus far, the third-generation artificial neural network model, known as spiking neural network (SNN), is regarded as the most viable option for implementation in neuromorphic hardware.[8,9] This is due to the fact that the synaptic devices comprising SNNs are equipped with spike timing-dependent plasticity (STDP), a property that enables information storage and processing by leveraging spike events that occur at distinct temporal points between pre- and post-synaptic neurons, thus enabling on-chip training and inference.[10,11]

Recent research in the field of neuromorphic hardware has focused on the implementation of artificial synapse devices using novel memory technologies, including resistive switching memristors,[12–14] phase-change memory (PCM),[15–17]

H. Yoon, S. Park, J. Baek, S. Yun, H. Son, J. Choi, D.-H. Kang
Department of Electrical Engineering and Computer Science (EECS)
Gwangju Institute of Science and Technology (GIST)
Gwangju 61005, Republic of Korea
E-mail: donghokang@gist.ac.kr

The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/adfm.202519498

DOI: 10.1002/adfm.202519498

S. Park, D.-H. Kang
Department of Semiconductor Engineering
Gwangju Institute of Science and Technology (GIST)
Gwangju 61005, Republic of Korea

Y. K. Kim, K. H. Kim, B. C. Jang
School of Electronic and Electrical Engineering
Kyungpook National University
Daegu 41566, Republic of Korea
E-mail: bc.jang@knu.ac.kr

B. C. Jang
School of Semiconductor Convergence Engineering
Kyungpook National University
Daegu 41566, Republic of Korea

ferroelectric field-effect transistors (FeFETs),[18–20] and electrochemical RAM (ECRAM).[21,22] These synaptic devices have successfully implemented essential functions such as long-term potentiation (LTP) and long-term depression (LTD). However, the target recognition and classification accuracy of neural networks based on these devices generally fail to reach the ideal accuracy achieved using software-based synaptic devices (see Table S1, Supporting Information,[18,23–27]). This limitation arises from the inherent inability of generating both positive and negative postsynaptic currents (PSCs) within a single synaptic device. Recent proposed synapse devices typically modulate current levels unidirectionally,[28] thereby enabling synaptic weight updates to only one polarity (positive or negative PSC). Consequently, the dynamic range of the synaptic device (defined as the difference between maximum and minimum conductances; $G_{max} - G_{min}$) can only be enhanced by increasing G_{max}, thereby constraining the improvement of neural network accuracy. Therefore, hardware implementations typically adopt a dual-synapse architecture, pairing two synaptic devices to represent positive and negative synaptic weights, respectively.[29,30] While this approach enables the representation of a full range of synaptic weights, dual-synapse architectures require additional peripheral circuits (e.g., subtractor), resulting in increased power consumption and circuit complexity.[28] Hence, the creation of a single synaptic device that can generate both positive and negative PSCs is crucial for achieving energy-efficient and scalable neuromorphic hardware.

In this paper, we demonstrate an optoelectronic synaptic device based on a van der Waals heterostructure that can generate both positive and negative PSCs, denoted as "bidirectional plasticity", by reversing the flow of photogenerated carriers under light irradiation. Our synaptic device is implemented by a rhenium disulfide (ReS_2)/tungsten diselenide (WSe_2) heterostructure as the channel layer and an oxygen-treated hexagonal boron nitride (*h*-BN) as the weight control layer (WCL). The proposed device enables tunable band bending via gate modulation, thereby enabling sign-switchable photocurrent. The bidirectional plasticity of our synaptic device relied on two distinct mechanisms: *(i)* immediate and reversible modulation of photocurrent polarity enabled by energy band bending of ReS_2/WSe_2 channels, and *(ii)* quasi-p-type or quasi-n-type doping phenomenon for WSe_2 layer attributed to photogenerated charge trapped in the oxygen-treated *h*-BN layer. As a result, in the theoretically implemented SNN, this bidirectional plasticity enables a face recognition accuracy of over 95%, which is more than 20% higher than that of unidirectional synaptic devices and comparable to that using software-based ideal synapses.

2. Results and Discussion

2.1. SNNs Based on ReS_2/WSe_2/*h*-BN Optoelectronic Synaptic Devices with Bidirectional Plasticity

Figure 1a depicts the schematic of two biological neurons connected by synapse through axon terminal of a presynaptic neuron and the dendritic membrane of a postsynaptic neuron. Upon the propagation of an action potential to the presynaptic axon terminal, the synapse is triggered, thereby facilitating the release of neurotransmitters that subsequently interact with the postsynaptic neuron. In this context, the synapse can function as either an excitatory or an inhibitory synapse, thereby increasing or decreasing the activity of the postsynaptic neuron, respectively. Here, synapses have "synaptic weights" that represent the strength of the connections between two neurons, and these weights determine the timing of electrical signal firing in the postsynaptic neuron. The modulation of these synaptic weights, also called synaptic plasticity, plays an important role in learning and memory in neural networks. To implement SNNs in hardware level, it is important to develop the synaptic device that mimics synaptic weight and synaptic plasticity. Hence, to implement SNNs at the hardware level, it is important to successfully develop synapse devices that mimic the roles of biological synapses (i.e., synaptic weights and plasticity). Figure 1b presents a conceptual diagram of a hardware SNN, constructed based on synaptic devices with conductance modulation characteristics expressed as synaptic weights (W). In this diagram, each presynaptic spike ($V_{i,j}$) triggers an input signal that passes through the synaptic device, where the magnitude of the signal is modulated by the conductance state ($G_{i,j}$) of the synaptic device. These modulated signals are subsequently integrated by the postsynaptic neuron, resulting in the expression $\sum G_{i,j}V_{i,j}$. When the accumulated signals exceed a predefined threshold, the postsynaptic neuron emits an output spike. Here, the timing difference between presynaptic and postsynaptic spikes induces synaptic weight updates, which is known as STDP.

In this paper, we propose a van der Waals heterostructure-based optoelectronic synaptic device capable of generating both positive and negative PSCs by modulating the polarity of the photogenerated current according to the voltage input through WCL. Figure 1c illustrates the schematic of our optoelectronic synapse, which consists of a ReS_2/WSe_2 heterojunction channel stacked on O_2 plasma-treated *h*-BN WCL (see the optical microscope image of the fabricated device in Figure S1, Supporting Information). Here, we designed the device structure that ReS_2 layer partially covers the WSe_2 channel. This partial overlap enhances the local vertical electric field and induces pronounced energy band bending at the ReS_2/WSe_2 heterojunction. When light is irradiated on the channel, photogenerated carriers are separated according to the built-in electric field at ReS_2/WSe_2 junction and collected at the pre- and post-synaptic terminals (source and drain terminals), resulting in the generation of photocurrent. Here, WCL is in contact with the WSe_2 layer, and the Fermi level of WSe_2 can be controlled by applying a gate voltage (V_G). Compared to ReS_2, WSe_2 has a Fermi level relatively close to the mid-gap,[31] thereby enabling considerable modulation of the Fermi level by electrostatic doping through V_G. This Fermi level modulation affects the strength and direction of the built-in electric field at the ReS_2/WSe_2 junction, generating a bidirectional photocurrent: i) Under the negative V_G, holes are accumulated in the WSe_2 layer, which modulates the Fermi level toward the valence band of WSe_2. This forms a built-in electric field in the direction from ReS_2 to WSe_2. Consequently, photogenerated electrons flow from the source to the drain, forming a positive drain current (I_D). ii) Conversely, the positive V_G shifts the WSe_2 Fermi level toward the conduction band. This creates a built-in electric field in the opposite direction and generates a negative drain current ($-I_D$). The electrical behavior of the device is conceptually illustrated in Figure 1d, where the output current reverses direction depending on the polarity of the applied gate voltage.

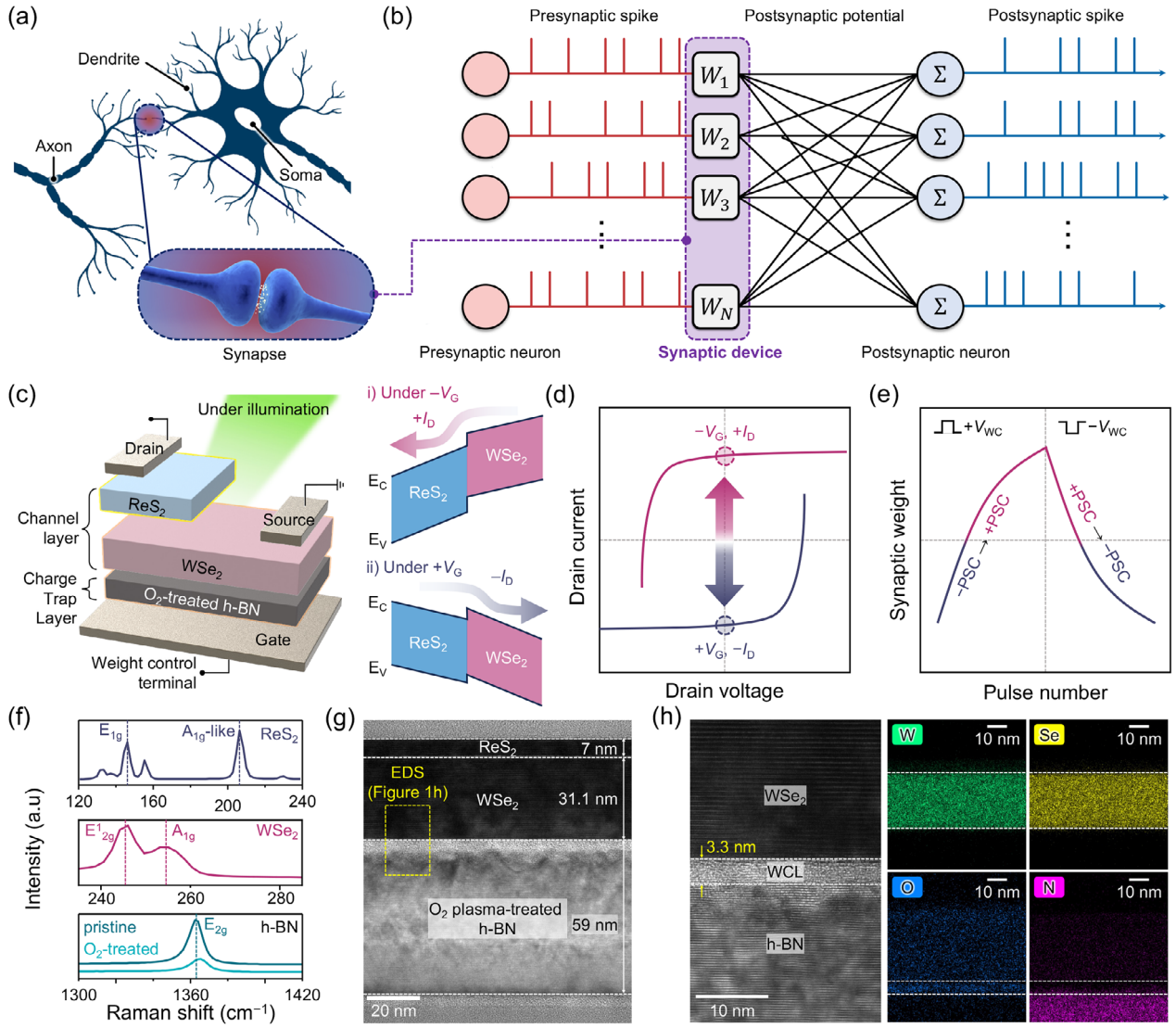

Figure 1. SNNs based on ReS_2/WSe_2/*h*-BN optoelectronic synaptic devices with bidirectional plasticity. a) Illustration of biological synapse with pre- and post-synaptic neurons. b) The SNN architecture incorporated with synaptic device. c) Schematic illustration of ReS_2/WSe_2/*h*-BN optoelectronic synaptic device (left) and energy band diagram of ReS_2/WSe_2 heterojunction i) under $-V_G$ and ii) under $+V_G$. Representative d) current-voltage and e) LTP/LTD characteristics of bidirectional optoelectronic synaptic device. f) Raman spectra of ReS_2 (upper panel), WSe_2 (middle panel) and *h*-BN (lower panel) measured from ReS_2/WSe_2/*h*-BN heterostructure. g) Cross-sectional TEM image of ReS_2/WSe_2/*h*-BN heterostructure. The scale bar in TEM image is 20 nm. h) High-resolution TEM image of WSe_2/WCL/*h*-BN heterostructure (left) and EDS elemental mapping images for tungsten, selenium, oxygen, and nitrogen. The scale bar in TEM and EDS images is 10 nm.

For the synaptic device operation, we employed O_2 plasma-treated *h*-BN layer as the WCL, where the trap sites in the O_2 plasma-treated *h*-BN layer can capture photogenerated electrons or holes. This phenomenon contributes to the long-term sustaining of the electrostatic doping effect on the WSe_2 layer (quasi-doping), thereby facilitating the generation of a bidirectional PSC. Figure 1e shows the representative synaptic characteristics of our device under light exposure. When positive weight control voltage (V_{WC}) spikes are applied to the gate terminal, electrons in the WSe_2 channel become trapped at the WCL trap sites, which induces pseudo-p-type doping in the WSe_2. This results in a gradual shift of the Fermi level of WSe_2 toward the valence band as the V_{WC} spike is continuously applied, leading to a transition from negative PSC to positive PSC in the LTP curve. Conversely, negative V_{WC} spikes capture holes from the WSe_2 channel into the WCL trap sites, leading to a gradual increase in the pseudo-n-type doping level with V_{WC} spike application. This results in a transition from positive to negative PSC in the LTD curve. The LTP/LTD characteristics of our synaptic device are similar to those of conventional optoelectronic synaptic devices (see Table S2, Supporting Information[32–38]); however, the key distinction is the directional reversal of the PSC. This enables bidirectional synaptic weight modulation (positive and negative conductance states) within a single device, thereby improving the learning efficiency of SNNs.

To investigate our optoelectronic synaptic devices in more detail, we performed Raman and cross-sectional transmission electron microscopy (TEM) analyses. Figure 1f presents the Raman spectra measured on ReS_2, WSe_2, and O_2 plasma-treated *h*-BN. We successfully observed characteristics Raman peaks of each layer: E_g (≈150 cm^{-1}) and A_g-like (≈210 cm^{-1}) modes in the ReS_2 layer,[39] $E^1{}_{2g}$ (≈248 cm^{-1}) and A_{1g} (≈251 cm^{-1}) modes in the WSe_2 region,[40] and E_{2g} (≈1363 cm^{-1}) modes in the *h*-BN layer.[41] In case of O_2 plasma-treated *h*-BN layer, the Raman spectrum exhibits a noticeable red shift and reduced peak intensity, indicating the presence of structural defects caused by partial oxidation. Figure 1g shows the cross-sectional TEM images of the $ReS_2/WSe_2/O_2$ plasma-treated *h*-BN heterostructure, where the thicknesses of the ReS_2, WSe_2, and O_2 plasma-treated *h*-BN are 7, 31.1, and 59 nm, respectively. We observed clean interfaces at the ReS_2/WSe_2 and WSe_2/O_2 plasma-treated h-BN due to the dangling-bond-free nature of van der Waals materials. In addition, as seen in Figure 1h, we further performed an energy-dispersive X-ray spectroscopy (EDS) mapping analysis near the WCL of the synaptic device to investigate the atomic compositions of the WSe_2/WCL/*h*-BN region. In the WCL (thickness: 3.3 nm), signals related to the oxygen element appeared clearly, but signals related to nitrogen, tungsten, and selenium were not present. Additional EDS spectrum profiles and X-ray photon spectroscopy (XPS) analyses (see Figures S2 and S3, Supporting Information) indicate that O_2 plasma treatment displaces nitrogen atoms from *h*-BN layer, resulting in the oxidized boron formation.[42]

2.2. Electrical Characteristics of ReS_2/WSe_2/*h*-BN Optoelectronic Device

Figure 2 presents the bidirectional operation and its mechanism of ReS_2/WSe_2/*h*-BN optoelectronic device. When the laser (λ = 532 nm ≈ 2.33 eV, P_{light} = 2 mW cm^{-2}) is exposed onto the ReS_2/WSe_2 channel (shown in Figure 2a), electrons in the valence band of the channel layer obtain photon energy sufficient to overcome the band gap (ReS_2 = ≈1.45 eV,[43] WSe_2 = ≈1.2 eV[44]), enabling them to be excited to the conduction band. This process generates electron-hole pairs, which are separated by the built-in electric field at the ReS_2/WSe_2 junction, contributing to the generation of photocurrent. Here, the built-in electric field at the ReS_2/WSe_2 junction can be controlled by modulating the WSe_2 Fermi level via gate-voltage-induced electrostatic doping. Figure 2b shows the I_D–V_G characteristics of the ReS_2/WSe_2/*h*-BN optoelectronic device with/without laser exposure. Under laser exposure, a positive drain current was measured at a gate voltage of –2 V, indicating that electrons flow from the source to the drain terminals. Subsequently, as the gate voltage increased to 2 V, the drain current gradually decreased, switching to a negative direction at V_G = –0.8 V, indicating electrons flow from the drain to the source terminals. This current polarity reversal phenomenon was only observed in the drain current (see Figure 2c), while the gate current maintained a constant noise level across the entire gate voltage range (see Figure S4, Supporting Information for log-scale plot of I_D–V_G curve). These results suggest that the observed directional reversal is not due to gate leakage but rather arises from electrostatic control that effectively reverses the built-in electric field within the heterojunction. Figure 2d shows the I_D–V_D characteristics by applying a gate voltage ranging from –5 V to 5 V with a step of 2.5 V. As the gate voltage is swept from –5 to 5 V, the output characteristics exhibit a clear polarity reversal in the drain current (+I_D at V_G = –5 V and –I_D at V_G = 5 V). This behavior highlights the bidirectional operational characteristics of ReS_2/WSe_2/*h*-BN optoelectronic device.

Next, to further investigate van der Waals heterostructure design for implementing bidirectional operation characteristics, we fabricated four optoelectronic devices based on heterostructures utilizing different types of 2D semiconducting materials ($MoS_2/ReSe_2$, $ReS_2/ReSe_2$, MoS_2/WSe_2, and WSe_2/ReS_2). Figure 2e shows the schematics of four optoelectronic devices, which share a common structure consisting of an *h*-BN insulator and a Si substrate but differ in the selection and order of the channel layers. These van der Waals heterostructures consists of 2D materials for which the bandgap is smaller than the photon energy of the 532 nm laser (E_{ph} = ≈2.33 eV), thereby facilitating the generation of photocarriers (see Figure S5, Supporting Information for details[45–47]). Figure 2f–i shows the output characteristics of optoelectronic devices based on the $MoS_2/ReSe_2$, $ReS_2/ReSe_2$, MoS_2/WSe_2, and WSe_2/ReS_2 heterostructures stacked on *h*-BN layer. In the cases of $MoS_2/ReSe_2$ (Figure 2f) and $ReS_2/ReSe_2$ (Figure 2g), a positive drain current is observed for positive V_D across the entire V_G range, while a negative drain current appears for negative V_D. This result suggests that only a conventional photoconductive effect is present, as the heterojunctions cannot generate sufficiently strong built-in electric fields required for the photovoltaic effect. Conversely, the MoS_2/WSe_2 heterostructure (Figure 2h) demonstrates a polarity reversal in the drain current at V_G = 0 and V_D = 0, indicating that *i)* this combination also establishes a sufficiently strong built-in electric field to enable the photovoltaic effect, and *ii)* the Fermi level of WSe_2 is effectively modulated via gate-induced electrostatic doping, resulting in behavior similar to that of the ReS_2/WSe_2 combination (Figure 2d). The slight variation in drain current magnitude is expected to attributable to the intrinsic differences in the optical absorption characteristics of MoS_2 and ReS_2. The output characteristics of the WSe_2/ReS_2 heterojunction device (Figure 2i) further emphasize the critical role of the WSe_2 layer in enabling Fermi level modulation via gate voltage. This heterostructure is a reversal of the stacking sequence compared to the ReS_2/WSe_2 device (Figure 2d), with the gate terminal close to the ReS_2 layer. In this case, a substantial reversal in the polarity of the drain current is not observed. This phenomenon can be attributed to the strong n-doping of ReS_2 induced by sulfur vacancies, which positions the Fermi level near the conduction band of ReS_2.[48] Consequently, gate voltage-induced electrostatic doping is impeded from effectively controlling the Fermi level of ReS_2.

Next, to further investigate the mechanism for the gate-tunable bidirectional photocurrent in the ReS_2/WSe_2/*h*-BN optoelectronic device, we conducted the Technology Computer-Aided Design (TCAD) simulations to analyze the energy band diagram of the ReS_2/WSe_2 heterojunction under various gate voltage conditions. Figure 2j shows the energy band diagram of ReS_2/WSe_2 heterojunction under the application of gate voltages of –5, 0, and 5 V (key parameters for TCAD simulations are in Figure S6, Supporting Information). This result demonstrates that significant energy band bending can be achieved even within a gate voltage

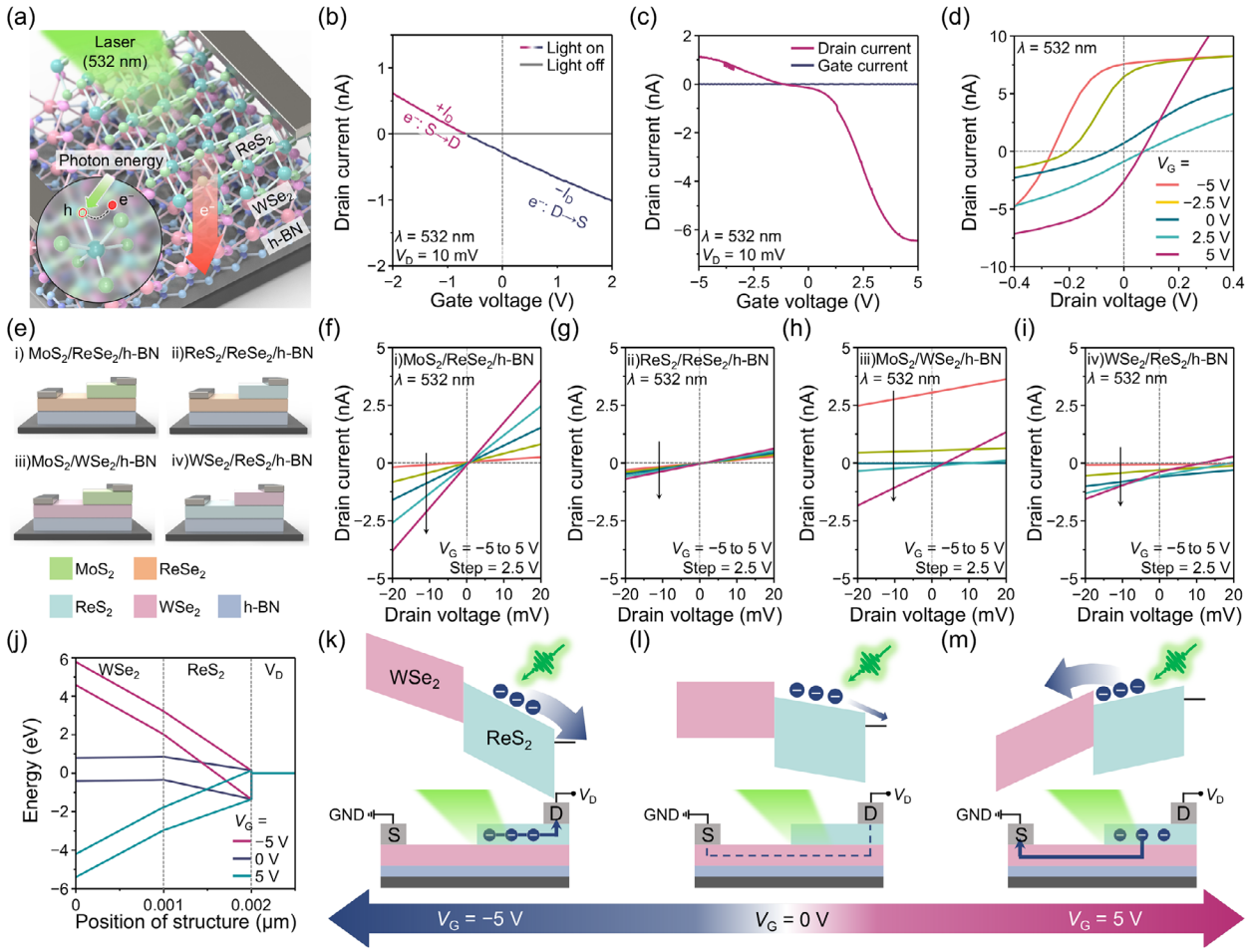

Figure 2. Electrical characteristics of $ReS_2/WSe_2/h$-BN optoelectronic device. a) Schematic illustration of photocarrier generation in $ReS_2/WSe_2/h$-BN optoelectronic device under 532 nm laser illumination. b) I_D–V_G characteristics of $ReS_2/WSe_2/h$-BN optoelectronic device with and without 532 nm laser exposure. c) Drain current and gate leakage of $ReS_2/WSe_2/h$-BN optoelectronic device under 532 nm laser exposure. d) Output characteristics of $ReS_2/WSe_2/h$-BN optoelectronic device under 532 nm laser exposure. e) Schematic diagrams optoelectronic devices based on various heterostructure configurations: (i) $MoS_2/ReSe_2/h$-BN, (ii) $ReS_2/ReSe_2/h$-BN, (iii) $MoS_2/WSe_2/h$-BN, and (iv) $WSe_2/ReS_2/h$-BN. Current-voltage characteristics of f) $MoS_2/ReSe_2/h$-BN, g) $ReS_2/ReSe_2/h$-BN, h) $MoS_2/WSe_2/h$-BN, and i) $WSe_2/ReS_2/h$-BN devices under 532 nm laser illumination with varying gate voltage application (V_G = –5 to 5 V). j) Energy band bending simulation of WSe_2/ReS_2 heterostructure carried out by TCAD. Photogenerated carrier dynamics in ReS_2/WSe_2 heterojunction under k) V_G = –5 V, (l) V_G = 0 V, and (m) V_G = 5 V.

range of ±5 V, enabling gate-tunable separation of photocarriers in opposite directions. Figure 2k–m provide a comprehensive explanation of the photocarrier flow under each gate voltage condition. When a negative gate voltage (V_G = –5 V) is applied (see Figure 2k), hole accumulation occurs in the WSe_2 layer, resulting in electrostatic p-doping. This results in a shift of Fermi level of WSe_2 toward the valence band, thereby forming a strong built-in electric field propagating from ReS_2 to WSe_2 at ReS_2/WSe_2 junction. This electric field governs the photogenerated carriers flowing toward the drain electrode (contacted with ReS_2 side), thereby contributing to the positive photocurrent. This built-in electric field persists even at V_G = 0 V (Figure 2l), resulting in maintaining generation of positive photocurrent (see V_G = 0 V case in Figure 2d). Conversely, applying a positive gate voltage (V_G = 5 V) induces electrostatic n-doping in the WSe_2 layer due to electron accumulation (Figure 2m), which shifts the Fermi level toward the conduction band and reverses the built-in electric field direction. This reversal drives photogenerated carriers from ReS_2 toward WSe_2, resulting in a negative photocurrent. Such gate-dependent reversal of photogenerated carrier flow explains the bidirectional photocurrent behavior observed in Figure 2d. These findings indicate that the bidirectional photocurrent arises from gate-induced modulation of the WSe_2 Fermi level, highlighting the critical role of the WSe_2 layer in enabling polarity in our $ReS_2/WSe_2/h$-BN optoelectronic device.

2.3. Synaptic Characteristics of $ReS_2/WSe_2/h$-BN Optoelectronic Synaptic Device

Figure 3 presents the synaptic characteristics of $ReS_2/WSe_2/h$-BN optoelectronic synaptic device with bidirectional PSCs under 532 nm laser exposure (P_{light} = 25 mW cm^{-2}). Figure 3a,b shows the dynamic photocurrent characteristics of $ReS_2/WSe_2/h$-BN

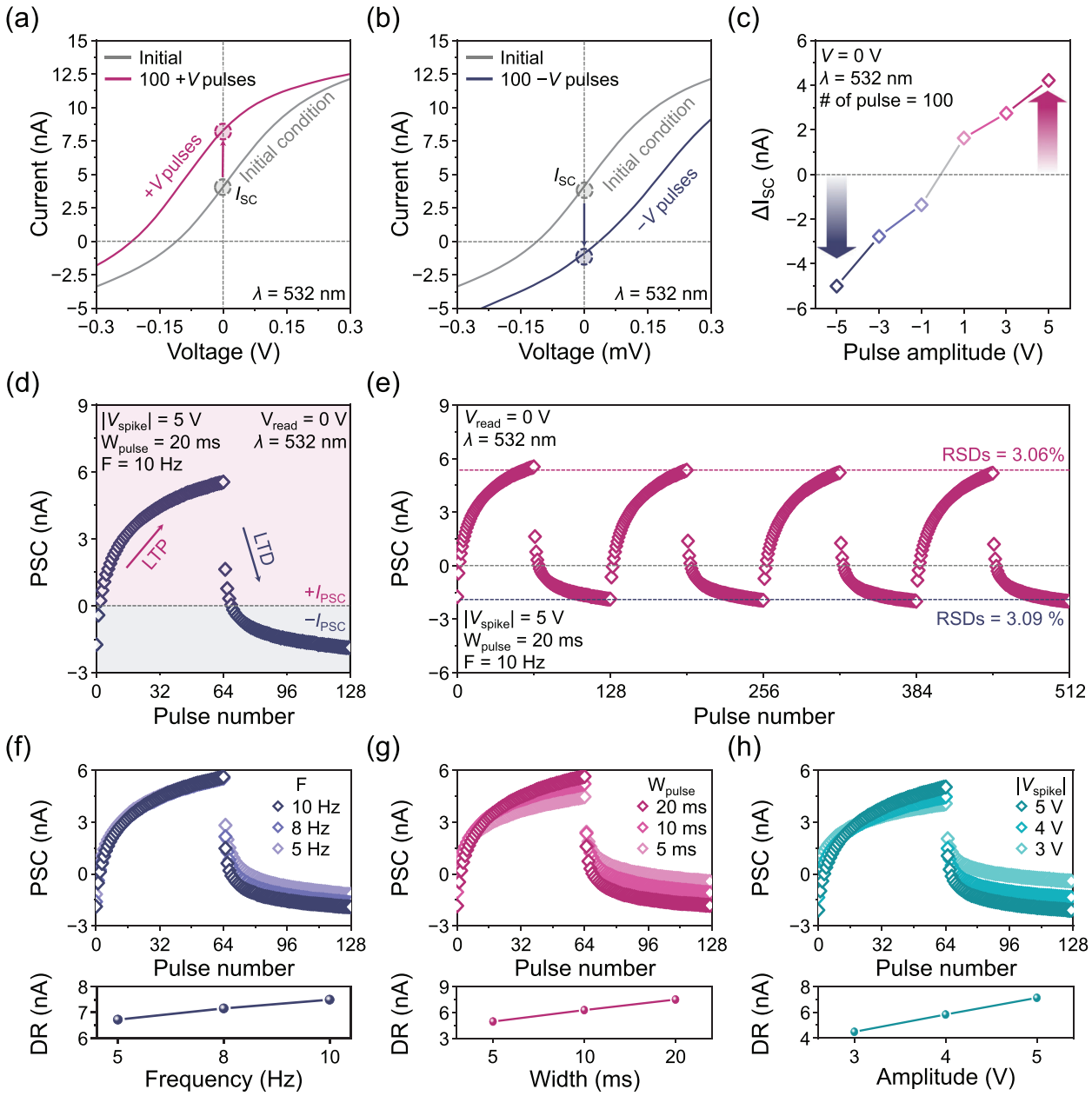

Figure 3. Synaptic characteristics of $ReS_2/WSe_2/h$-BN optoelectronic synaptic device. Current-voltage characteristics of $ReS_2/WSe_2/h$-BN optoelectronic synaptic device before and after a) 100 +*V* pulses and b) 100 –*V* pulses applied to the V_{WC}. c) Short-circuit current changes (ΔI_{SC}) as a function of voltage pulse amplitude (after 100 programming pulses). d) Representative LTP/LTD curve under sequential excitatory/inhibitory pulses ($|V_{spike}|$ = 5 V, W_{pulse} = 20 ms, F = 10 Hz), exhibiting bidirectional PSC responses. e) Four consecutive LTP/LTD cycles (64 potentiating and 64 depressing pulses per cycle; $|V_{spike}|$ = 5 V, W_{pulse} = 20 ms, F = 10 Hz) measured from $ReS_2/WSe_2/h$-BN optoelectronic synaptic device. LTP/LTD characteristics and extracted dynamic range (DR) depended on f) pulse frequency (5–10 Hz), g) pulse width (5–20 ms), and h) pulse amplitude (3–5 V).

optoelectronic synaptic device. Under 532 nm laser illumination, our optoelectronic synaptic device initially shows an obvious photovoltaic effect with short-circuit current (I_{SC}) of 4.1 nA and open-circuit voltage (V_{OC}) of –0.11 V. After 100 of positive voltage pulse programming (+5 V, 200 ms) to the weight control terminal (V_{WC}, same as gate voltage terminal), the device showed current-voltage behavior with an enhanced I_{SC} of 8.3 nA and V_{OC} of –0.21 V (red line in Figure 3a). Similarly, the same device could be modulated with an opposite photovoltaic effect with an I_{SC} of –0.91 nA and V_{OC} of 0.03 V after 100 of negative voltage pulse programming (–5 V, 200 ms) to the V_{WC} (blue line in Figure 3b). This current-voltage behavior also varied with the amplitude of the voltage pulse applied to V_{WC}. As shown in Figure 3c, increasing the pulse amplitude from 1 to 5 led to a more pronounced change in the short-circuit current (ΔI_{SC}). Notably, the direction of ΔI_{SC} consistently followed the polarity of the programmed pulse: negative pulses induced a negative shift in I_{SC}, while positive pulses resulted in a positive shift. Interestingly, the polarity of

ΔI_{SC} after voltage pulse programming is opposite to that observed in Figure 2d ($I_D > 0$ under $V_G < 0$, while $I_D < 0$ under $V_G > 0$). This phenomenon is attributed to charge trapping/detrapping in the defect states in WCL (i.e., O_2 plasma-treated *h*-BN layer), which induces a pseudo-doping effect in the WSe_2 layer that is opposite in polarity to the electrostatic doping by applying the gate bias. Under application of a positive (negative) voltage pulse, electrons (holes) will be captured by trap states at the O_2 plasma-treated *h*-BN layer. These trapped electrons (holes) electrostatically cause the WSe_2 channel to be pseudo-p-type (pseudo-n-type).[38,49] This results in a shift of the Fermi level of WSe_2 toward the valence band (conduction band), a phenomenon that persists even after the removal of the applied voltage pulse. As shown in Figure S7 (Supporting Information), the device without O_2 plasma treatment on *h*-BN surface exhibited no observable current modulation or LTP/LTD behavior, confirming that the plasma-induced charge-trapping sites are essential for synaptic functionality.

The non-volatile and bidirectional photocurrent dynamics of ReS_2/WSe_2/*h*-BN optoelectronic device makes it possible to emulate the synaptic characteristics by modulating the conductance in the ReS_2/WSe_2 channel layer with the application of voltage spike through V_{WC}. As shown in Figure S8 (Supporting Information), we could observe a distinct potentiation and depression operations under the application of two voltage spikes with amplitude (V_{spike}) of ±5 V, width (W_{pulse}) of 20 ms and frequency (F) of 10 Hz. Subsequently, we investigated the LTP/LTD characteristics of the optoelectronic synaptic device using PSC measurements under 532 nm laser illumination (P_{light} = 25 mW cm^{-2}). Figure 3d shows the representative LTP/LTD curve obtained from our optoelectronic synaptic device under the application of a sequence of excitatory/inhibitory pulses ($|V_{spike}|$ = 5 V, W_{pulse} = 20 ms, and F = 5 Hz). When 128 excitatory pulses were delivered, the PSC response (I_{PSC}) gradually increased from –1.74 to 5.5 nA. Conversely, the application of inhibitory pulses resulted in a decrease of I_{PSC} from 1.63 to –1.87 nA. It is important to note that positive and negative PSC responses were observed in both LTP and LTD curves. In addition, as shown in Figure S9 (Supporting Information), when both optical and electrical stimuli were completely removed during the LTP/LTD measurements, the synaptic device maintained its stored state. The PSC recovered immediately upon re-application of the stimuli, confirming that the memory state is retained even without continuous light illumination. Figure 3e shows the four cycles of the LTP/LTD curves corresponding to 512 pulses while applying consecutive 64 potentiating and 64 depressing pulses to the V_{WC} for a cycle ($|V_{spike}|$ = 5 V, W_{pulse} = 20 ms, and F = 10 Hz). Here, we could observe a stable and reliable bidirectional operation of the device, where the calculated relative standard deviations (RSDs) of the maximum and minimum I_{PSC} were 3.06% and 3.09%, respectively. Further stability test (10 cycles) and retention test of our synaptic device is shown in Figures S10 and S11 (Supporting Information).

Next, we measured the PSC by applying a variety of voltage pulse conditions. Figure 3f–h shows the LTP/LTD characteristics in terms of frequency, width, and amplitude along with dynamic range of the LTP/LTD curves. Unlike conventional synaptic device with unidirectional PSC response, our device demonstrates bidirectional PSC; therefore, the dynamic range was defined as the difference between the maximum and minimum PSC values. As shown in Figure 3f, frequency modulation from 5 to 10 Hz (with fixed W_{pulse} of 20 ms and $|V_{spike}|$ of 5 V) led to a slight increase in dynamic range from 6.72 nA to 7.49 nA. Similarly, as depicted in Figure 3g, varying the pulse width from 5 to 20 ms (with F and $|V_{spike}|$ fixed at 10 Hz and 5 V, respectively) resulted in an increase in dynamic range from 4.93 to 7.48 nA. In the case of pulse amplitude engineering, increasing $|V_{spike}|$ from 3 to 5 V (with F and W_{pulse} fixed at 10 Hz and 20 ms, respectively) yielded a gradual enhancement in dynamic range, from 4.47 to 7.5 nA, as shown in Figure 3h. For all pulse modulation schemes, the dynamic range consistently increased with higher-energy pulse sets. This is attributed to the accumulation of a larger number of carriers trapped in the WCL by the voltage pulses, which are retained within the WCL before the arrival of subsequent pulses. In addition, by increasing the laser power density from 2 to 25 mW cm^{-2}, we were able to achieve a more than 14-fold enhancement in PSC amplitude (from 0.52 to 7.5 nA), as shown in Figure S12 (Supporting Information). This indicates that the number of photogenerated carriers directly determines the PSC amplitude. Despite its excellent dynamic range, the device exhibited relatively poor non-linearity under most pulse conditions, resulting in substantial deviations from target values during synaptic weight updates. These cumulative errors, particularly in synapses with frequent weight changes, can significantly degrade the overall recognition accuracy of the neural network.[50] As shown in Figure S13 (Supporting Information), the non-linearity values for a representative LTP/LTD curve were 5.54 and 6.53, respectively (with values closer to 1 indicating higher linearity). This non-ideal behavior is expected to be due to the high density of trap sites formed in the O_2 plasma-treated *h*-BN layer, which leads to rapid saturation of charge trapping during the initial pulses. To improve the non-linearity of our device, we applied a pulse scheme with gradually varying amplitudes ($|V_{spike}|$ = 1.25 to 5 V, incremented or decremented by 1.25 V every 16 pulses). This approach led to a significant improvement in synaptic performance, reducing LTP and LTD non-linearity to 1.59 and 1.07, respectively. In Table S3 (Supporting Information), we provided a quantitative comparison between our synaptic device and recently reported high-performance optoelectronic synaptic devices.[38,51–58] The results confirm that our device exhibited competitive performance across key parameters, including PSC amplitude, dynamic range, linearity, and energy consumption. In addition, we fabricated seven devices for device-to-device analysis, all of which exhibited similar LTP/LTD characteristics (see Figure S14, Supporting Information) with RSDs of 11.2% and 10.35% for the maximum and minimum PSC levels, respectively. Further studies for improving both non-linearity and dynamic range for ReS_2/WSe_2/*h*-BN optoelectronic synaptic device is required, such as controlling the trap state density in WCL or optimizing wavelength and intensity of incident light conditions.

2.4. Facial Recognition using SNNs Based on ReS_2/WSe_2/*h*-BN Optoelectronic Synaptic Device

To demonstrate the feasibility for pattern recognition of our ReS_2/WSe_2/*h*-BN optoelectronic synaptic device, we performed

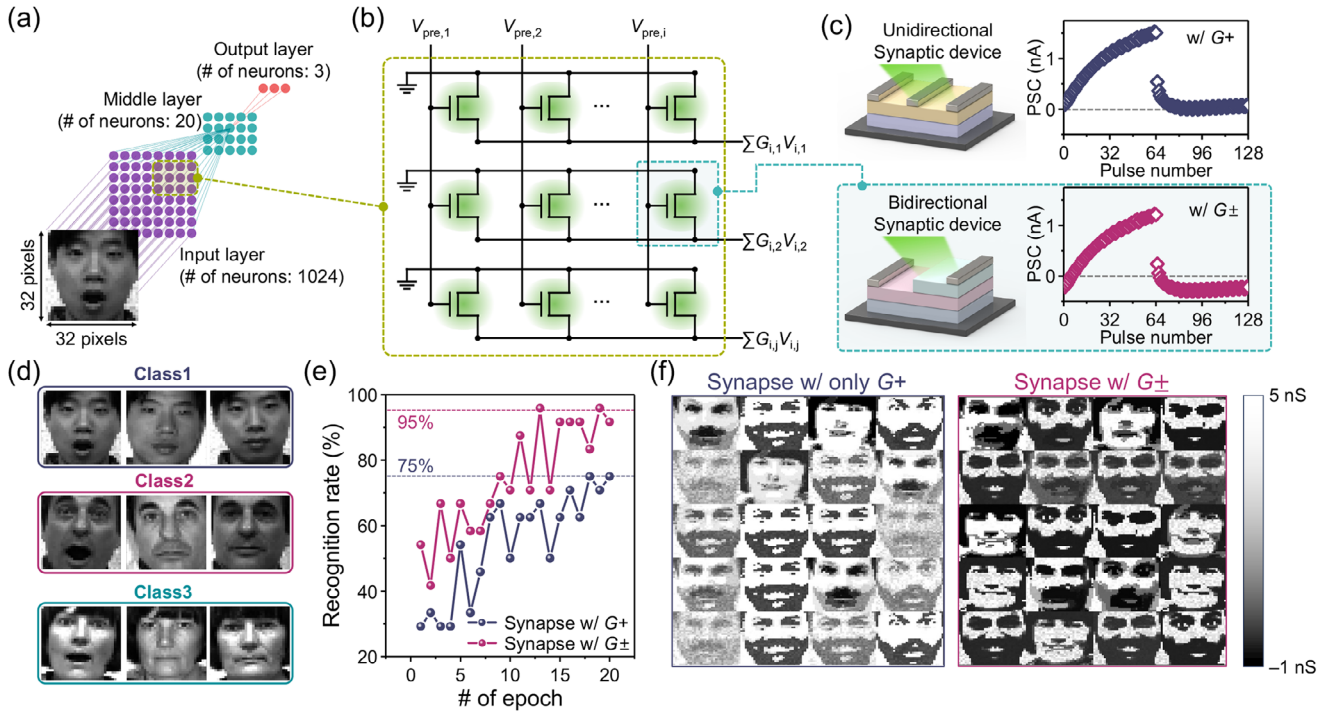

Figure 4. Facial recognition using SNNs based on $ReS_2/WSe_2/h$-BN optoelectronic synaptic device. a) Schematic of the SNN architecture utilizing the proposed $ReS_2/WSe_2/h$-BN optoelectronic synaptic device, consisting of 1024 input neurons, 20 hidden neurons, and 3 output neurons. b) Crossbar array implementation of the SNN. c) Unit cell in SNN with (upper panel) unidirectional synaptic device with G^+ and (lower panel) bidirectional synaptic device enabling both positive and negative synaptic weight expression (G^+/G^-). d) Input images of three identity classes used for unsupervised STDP-based training. e) Comparison of recognition accuracy as a function of training epochs, demonstrating superior learning performance with the bipolar G^+/G^- synapse. f) Visualization of final neuron outputs, highlighting clearer and more distinct class representation with the G^+/G^- synapse due to effective lateral inhibition.

a device-to-system level simulation framework that integrates our synapse device properties into SNN model. As illustrated in **Figure** 4a, the network architecture features a fully connected two-layer structure composed of 1024 input neurons, 20 hidden neurons, and three output neurons. A set of 32 × 32 grayscale facial images served as the input dataset for unsupervised learning, where each pixel intensity was assigned to a corresponding input node, and each output node represented a specific identity class. The synaptic connectivity was configured as a crossbar array (Figure 4b), with each junction incorporating the $ReS_2/WSe_2/h$-BN optoelectronic synaptic device. The crossbar architecture is considered an optimal hardware platform for implementing ANNs due to its support for key computational kernels. It inherently enables efficient vector–matrix multiplication (e.g., dot product), a fundamental operation in ANN. Additionally, this architecture allows parallel rank-1 weight updates, enabling winner-takes-all mechanisms essential for competitive learning.[59] Figure 4c presents a comparison of synaptic devices used in facial recognition simulations, featuring unidirectional PSC responses (upper panel) and bidirectional PSC responses (lower panel). Unlike conventional unidirectional synaptic devices restricted to the positive conductance regime (G^+), our synaptic device enables polarity-tunable PSCs that realize synaptic weight modulation in both positive (G^+) and negative (G^-) states. This functionality enables the implementation of single synapse device to represent positive and negative weights compared to conventional dual synapse configuration based on unidirectional synapse devices, as shown in the right panel of Figure 4c.

Nine training images extracted from the Yale Face Database for three human faces are shown in Figure 4d. A training image was applied into the SNN composed of optoelectronic synaptic devices, where each of the 1024 input neurons represented a pixel and generated spikes with rates proportional to pixel intensity (see Figure S15a, Supporting Information). These presynaptic spikes generated postsynaptic currents through conductance of synaptic devices, which were integrated by leaky integrate-and-fire neurons. Vector–matrix multiplication was inherently performed by the crossbar array architecture. The neuron receiving the highest integrated current fired, initiating synaptic updates through biphasic postsynaptic spikes. Depending on the spike timing difference (Δt), either $+V_{spike}$ or $-V_{spike}$ pulses were applied, resulting in a decrease or increase in synaptic conductance, respectively (see Figure S15b, Supporting Information). The SNN was trained via a simplified STDP learning rule scheme[25] by designing an appropriate timing correlation between the presynaptic and postsynaptic spikes. Unlike the complex, biologically inspired STDP scheme, the simplified STDP rule significantly reduces peripheral circuit complexity by eliminating the need for precise spike timing alignment. Based on the experimentally obtained LTD/LTD characteristics of the optoelectronic synaptic device, synaptic weight updates were modeled as

a function of pulse. Following training, the ANN was tested using 24 images from three individuals.

Figure 4e compares the face recognition accuracy over training epochs for networks employing synapses with bidirectional (G^+/G^-) versus unidirectional (G^+) synaptic weight modulation. The synaptic weight (G) used for simulation was optimized for balanced potentiation and depression responses (see Figure S16, Supporting Information). The network incorporating the bidirectional synaptic device achieved over 90% accuracy within 20 training epochs, reaching a maximum of 95%, whereas the unidirectional synapse plateaued below 75%. This contrast highlights the critical role of bidirectional synaptic weight modulation, which inherently supports a symmetric STDP learning rule and thereby enhances the representational and adaptive capabilities of the SNN. Further details can be found in Note 2 (Supporting Information). The large fluctuations in recognition rate are attributed to a well-kwon feature of SNN. In contrast to ANNs, where backpropagation is the standard training algorithm, SNNs typically employ STDP. However, this rule often results in unstable gradient updates and susceptibility to local minima, thereby leading to large fluctuations in recognition accuracy. Despite these fluctuations, our bidirectional synaptic device consistently outperforms its unidirectional counterpart, demonstrating the robustness of the observed improvement. The qualitative differences in learned outputs are visualized in Figure 4f, where networks with bidirectional synaptic device produce sharper, more class-distinct spiking patterns compared to the blurred and non-selective activity observed in the unidirectional case. In addition, the bidirectional synaptic device showed the improved recognition rate of ≈10% on the Modified National Institute of Standards and Technology (MNIST) handwritten digit dataset compared with its unidirectional synapse (Figure S17, Supporting Information). These results indicate that bidirectional PSC functionality is instrumental in realizing effective lateral inhibition and improved classification performance in neuromorphic systems. We also evaluated the device-to-device and cycle-to-cycle variability based on the recognition rate per training epoch of the SNN, as depicted in Figure S18 (Supporting Information), where error bars indicate the corresponding variations.

3. Conclusion

In this study, we demonstrated the $ReS_2/WSe_2/h$-BN optoelectronic synaptic device that intrinsically exhibits both positive and negative PSC modulation by reversing photocurrent polarity through gate bias and weight-control voltage pulses. This bidirectional plasticity originates from Fermi level modulation in the WSe_2 layer, induced by the pseudo-doping effect resulting from charge trapping in the WCL triggered by the application of voltage pulses through V_{WC}. Our device exhibited a sign-switchable photovoltaic response and robust, repeatable potentiation/depression of PSC response. The LTP/LTD characteristics of the $ReS_2/WSe_2/h$-BN optoelectronic synaptic device exhibited a dynamic range of up to 7.5 nA when driven by a high-energy pulse set (F = 10 Hz, W_{pulse} = 20 ms, and $|V_{spike}|$ = 5 V). Although the initial non-linearity of the LTP/LTD curves was relatively modest, it was significantly improved by adopting a gradually ramped pulse scheme, yielding non-linearity of 1.59 (LTP) and 1.07 (LTD). A similar study by Zhai et al.[60] reported gate-tunable bidirectional photoresponse for hardware convolution processing, whereas our work extends this concept to synaptic functionality, demonstrating light-assisted bidirectional PSC modulation and enhanced SNN learning performance. Furthermore, system-level simulations employing a 1024–20–3 SNN with a crossbar array confirmed the practical advantage of bidirectional synapses. Networks incorporating bidirectional (G^+/G^-) synapses achieving over 90% accuracy within 20 epochs and reaching a peak of 95%, whereas those using unidirectional (G^+) synapses plateaued below 75%. These results demonstrate that our polarity-switchable optoelectronic synaptic device can support online learning in hardware, offering a promising pathway toward scalable and energy-efficient neuromorphic systems.

4. Experimental Section

Fabrication of the $ReS_2/WSe_2/h$-BN Optoelectronic Synaptic Device: The *h*-BN flake was mechanically transferred on the 90 nm-thick SiO_2 oxide layer on heavily p-doped Si substrate using dry-transfer technique. To form the WCL, The O_2 plasma treatment process was carried out on the *h*-BN flake by a reactive ion etching (RIE) system (PLASMA LAB80) at an O_2 gas flow rate of 5 sccm, RF power of 5 W, and etching duration of 10 min. WSe_2 and ReS_2 flakes were then transferred onto the WCL/*h*-BN by using the same transfer technique. Source and drain electrodes (length and width of the channel area were 5 µm) were patterned on the $ReS_2/WSe_2/h$-BN sample using electron-beam lithography technique (Raith Elphy Quantum graphic writer) performed with a field-emission scanning electron microscope (SU5000). After patterning, 20-nm-thick Pt and 200-nm-thick Ag electrodes were deposited via electron-beam evaporation.

Material Characterization of ReS_2/WSe_2/WCL/h-BN Heterostructure: For the structural and elemental analyses of the ReS_2/WSe_2/WCL/*h*-BN heterostructure, focused ion beam (FIB) milling was performed using a Hitachi NX5000 system. The resulting lamella was then investigated using a Talos F200X G2 TEM operated at 200 kV. Raman spectra were obtained using a Horiba LabRAM HR Evolution with a 532 nm excitation laser operating at a power of 25 µW. The spectral resolution was ensured by employing a grating with a groove density of 1800 gr mm^{-1}. The XPS analysis was carried out by NEXSA G2 (Thermo Fisher Scientific) with minimum energy step size of 3 meV and spot size of <400 µm.

Electrical and Synaptic Characterization of the Device: The current–voltage (I_{DS}–V_{GS}) characteristics and synaptic responses were measured using a parameter analyzer (Keysight B2912B) and a waveform generator (Keysight 33500B) in a vacuum probe station (≈1×10^{-5} Torr). A continuous-wave 532 nm laser (LightHUB) with an optical power density of up to 50 mW cm^{-2} was used as the optical stimulus. The laser was applied in a free-space, normal-incidence configuration, illuminating the entire device channel area. Electrical spike signals for synaptic tests were applied to the gate terminal in the form of square pulses with controlled amplitude, frequency, and width. All electrical bias conditions are provided in the corresponding figure.

Energy Band and SNN Simulations: Energy band simulations were carried out using Synopsys Sentaurus (Synopsys Inc.), a TCAD software package. System-level SNN simulations for facial recognition were conducted in MATLAB. The device-to-system level SNN simulation framework, following the methodology reported in previous work was utilized.[25,61] The facial images shown in Figure 4 were sourced from the Yale Face Database, with full permission obtained in accordance with Yale's usage policy. These images were used to evaluate the classification performance of the SNN.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This research was supported by the National Research Foundation of Korea (NRF) grants (RS-2024-00355248) funded by Ministry of Science and ICT. This work was also supported by the Gwangju Institute of Science and Technology (GIST) research fund (Future-Leading Specialized Research Project, 2025). The authors would like to acknowledge and thank to the GIST Nanoinfra for Compound Semiconductors (G-NICS) for the device fabrication and GIST Advanced Institute of Instrumental Analysis (GAIA) for the Raman, TEM, and XPS analyses.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

H.Y., S.P., and Y.K.K. contributed equally to this work. H.Y., S.P., Y.K.K., B.C.J., and D.- H.K. conceived the work; H.Y., J.B., and D.-H.K. designed the experiments and analyzed the data; Y.K.K. and B.C.J. designed system-level SNN and conducted facial recognition simulation; S.P., H.S., and S.Y. fabricated devices; H.Y., S.P., J.B., and J.C. performed the device characterization; K.H.K. and B.C.J. conducted TCAD simulation; S.P. and H.S. performed TEM, Raman, and XPS analyses; H.Y., S.P., Y.K.K., B.C.J., and D.-H.K. prepared the manuscript. All authors have revised this manuscript. B.C.J. and D.-H.K. guided the entire project.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

bidirectional plasticity, neuromorphic computing, optoelectronic synapse, spiking neural network, van der Waals heterostructure

Received: July 28, 2025
Revised: October 8, 2025
Published online:

[1] J. Backus, *Commun. ACM* **1978**, *21*, 613.
[2] S. Yu, H. Jiang, S. Huang, X. Peng, A. Lu, *IEEE Circuits and Systems Magazine* **2021**, *21*, 31.
[3] C. X. Xue, Y. C. Chiu, T. W. Liu, T. Y. Huang, J. S. Liu, T. W. Chang, H. Y. Kao, J. H. Wang, S. Y. Wei, C. Y. Lee, S.-P. Huang, J.-M. Hung, S.-H. Teng, W.-C. Wei, Y.-R. Chen, T.-H. Hsu, Y.-K. Chen, Y.-C. Lo, T.-H. Wen, C.-C. Lo, R.-S. Liu, C.-C. Hsieh, K.-T. Tang, M.-S. Ho, C.-Y. Su, C.-C. Chou, Y.-D. Chih, M.-F. Chang, *Nat. Electron.* **2020**, *4*, 81.
[4] W. Wan, R. Kubendran, C. Schaefer, S. B. Eryilmaz, W. Zhang, D. Wu, S. Deiss, P. Raina, H. Qian, B. Gao, S. Joshi, H. Wu, H.-S. Philip Wong, G. Cauwenberghs, *Nature* **2022**, *608*, 504.
[5] W. Haensch, A. Raghunathan, K. Roy, B. Chakrabarti, C. M. Phatak, C. Wang, S. Guha, *Adv. Mater.* **2023**, *35*, 2204944.
[6] C. Mead, *Proc. IEEE* **1990**, *78*, 1629.
[7] D. Kudithipudi, C. Schuman, C. M. Vineyard, T. Pandit, C. Merkel, R. Kubendran, J. B. Aimone, G. Orchard, C. Mayr, R. Benosman, J. Hays, C. Young, C. Bartolozzi, A. Majumdar, S. G. Cardwell, M. Payvand, S. Buckley, S. Kulkarni, H. A. Gonzalez, G. Cauwenberghs, C. S. Thakur, A. Subramoney, S. Furber, *Nature* **2025**, *637*, 801.
[8] M. Davies, N. Srinivasa, T.-H. Lin, G. Chinya, Y. Cao, S. H. Choday, G. Dimou, P. Joshi, N. Imam, S. Jain, Y. Liao, C.-K. Lin, A. Lines, R. Liu, D. Mathaikutty, S. McCoy, A. Paul, J. Tse, G. Venkataramanan, Y.-H. Weng, A. Wild, Y. Yang, H. Wang, *IEEE Micro* **2018**, *38*, 82.
[9] S. B. Furber, F. Galluppi, S. Temple, L. A. Plana, *Proc. IEEE* **2014**, *102*, 652.
[10] G. Q. Bi, M. M. Poo, *J. Neurosci.* **1998**, *18*, 10464.
[11] N. Caporale, Y. Dan, *Annu. Rev. Neurosci.* **2008**, *31*, 25.
[12] A. Valentian, F. Rummens, E. Vianello, T. Mesquida, C. L. M. de Boissac, O. Bichler, C. Reita, *Proceedings of the International Electron Devices Meeting (IEDM)* IEEE, San Francisco, CA **2019**.
[13] Y. Wang, T. Tang, L. Xia, T. Mesquida, C. L. M. de Boissac, O. Bichler, C. Reita, *Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, IEEE, San Francisco, CA, **2015**, pp. 189–194.
[14] J. Park, A. Kumar, Y. Zhou, S. Oh, J.-H. Kim, Y. Shi, S. Jain, G. Hota, E. Qiu, A. L. Nagle, I. K. Schuller, C. D. Schuman, G. Cauwenberghs, D. Kuzum, *Nat. Commun.* **2024**, *15*, 3492.
[15] T. Ortner, H. Petschenig, A. Vasilopoulos, R. Renner, Š. Brglez, T. Limbacher, E. Piñero, A. Linares-Barranco, A. Pantazi, R. Legenstein, *Nat. Commun.* **2025**, *16*, 1243.
[16] M. Le Gallo, R. Khaddam-Aljameh, M. Stanisavljevic, A. Vasilopoulos, B. Kersting, M. Dazzi, G. Karunaratne, M. Brändli, A. Singh, S. M. Müller, J. Büchel, X. Timoneda, V. Joshi, M. J. Rasch, U. Egger, A. Garofalo, A. Petropoulos, T. Antonakopoulos, K. Brew, S. Choi, I. Ok, T. Philip, V. Chan, C. Silvestre, I. Ahsan, N. Saulnier, V. Narayanan, P. A. Francese, E. Eleftheriou, A. Sebastian, *Nat. Electron.* **2023**, *6*, 680.
[17] V. Joshi, M. Le Gallo, S. Haefeli, I Boybat, SR Nandakumar, C Piveteau, M Dazzi, B Rajendran, A. Sebastian, E. Eleftheriou, *Nat. Commun.* **2020**, *11*, 2473.
[18] H. Choi, S. Baek, H. Jung, T. Kang, S. Lee, J. Jeon, B. C. Jang, S. Lee, *Adv. Mater.* **2025**, *37*, 2406970.
[19] I. J. Kim, M. K. Kim, J. S. Lee, *Nat. Commun.* **2023**, *14*, 504.
[20] Y. Chen, Y. Zhou, F. Zhuge, B. Tian, M. Yan, Y. Li, Y. He, X. S. Miao, *npj 2D Mater. Appl.* **2019**, *3*, 31.
[21] A. A. Talin, Y. Li, D. A. Robinson, E. J. Fuller, S. Kumar, *Adv. Mater.* **2023**, *35*, 2204771.
[22] P. Chen, F. Liu, P. Lin, P. Li, Y. Xiao, B. Zhang, G. Pan, *Nat. Commun.* **2023**, *14*, 6184.
[23] T. Hynnä, A. Schulman, V. Lähteenlahti, H. Huhtinen, P. Paturi, *ACS Appl. Electron. Mater.* **2024**, *6*, 292.
[24] Y. K. Kim, S. Park, J. Choi, H. Park, B. C. Jang, *Adv. Funct. Mater.* **2024**, *34*, 2405670.
[25] B. C. Jang, S. Kim, S. Y. Yang, J. Park, J.-H. Cha, J. Oh, J. Choi, S. G. Im, V. P. Dravid, S.-Y. Choi, *Nano Lett.* **2019**, *19*, 839.
[26] J. B. Roldan, D. Maldonado, C. Aguilera-Pedregosa, E. Moreno, F. Aguirre, R. Romero-Zaliz, A. M. García-Vico, Y. Shen, M. Lanza, *npj 2D Mater. Appl.* **2022**, *6*, 63.
[27] Q. Duan, Z. Jing, X. Zou, Y. Wang, K. Yang, T. Zhang, S. Wu, R. Huang, Y. Yang, *Nat. Commun.* **2020**, *11*, 3399.
[28] D. Ielmini, S. Ambrogio, *Nanotechnology* **2019**, *31*, 092001.
[29] S. Oh, J. I. Cho, B. H. Lee, S. Seo, J. H. Lee, H. Choo, K. Heo, S. Y. Lee, J. H. Park, *Sci. Adv.* **2021**, *7*, abg9450.
[30] S. Oh, S. Jung, M. H. Ali, J. H. Kim, H. Kim, J. H. Park, *ACS Appl. Mater. Interfaces* **2020**, *12*, 38299.
[31] F. Ali, F. Ahmed, M. Taqi, S. B. Mitta, T. D. Ngo, D. J. Eom, K. Watanabe, T. Taniguchi, H. Kim, E. Hwang, W. J. Yoo, *2D Mater.* **2021**, *8*, 035027.
[32] Y. X. Hou, Y. Li, Z. C. Zhang, J. Q. Li, D. H. Qi, X. D. Chen, J. J. Wang, B. W. Yao, M. X. Yu, T. B. Lu, J. Zhang, *ACS Nano* **2021**, *15*, 1497.
[33] R. Yang, Y. Wang, S. Li, D. Hu, Q. Chen, F. Zhuge, Z. Ye, X. Pi, J. Lu, *Adv. Funct. Mater.* **2024**, *34*, 2312444.
[34] M. Xu, T. Xu, A. Yu, H. Wang, H. Wang, M. Zubair, M. Luo, C. Shan, X. Guo, F. Wang, W. Hu, Y. Zhu, *Adv. Opt. Mater.* **2021**, *9*, 2100937.

[35] Y. Chen, M. Zhang, D. Li, Y. Tang, H. Ren, J. Li, K. Liang, Y. Wang, L. Wen, W. Li, W. Kong, S. Liu, H. Wang, D. Wang, B. Zhu, *ACS Nano* **2023**, *17*, 12499.
[36] X. Zhu, C. Gao, Y. Ren, X. Zhang, E. Li, C. Wang, F. Yang, J. Wu, W. Hu, H. Chen, *Adv. Mater.* **2023**, *35*, 2301468.
[37] C.-M. Yang, T.-C. Chen, D. Verma, L.-J. Li, B. Liu, W.-H. Chang, C.-S. Lai, *Adv. Funct. Mater.* **2020**, *30*, 2001598.
[38] H. Ahn, Y. Kim, S. Seo, J. Lee, S. Lee, S. Oh, B. Kim, J. Park, S. Kang, Y. Kim, A. Ham, J. Lee, D. Park, S. Kwon, D. Lee, J.-E. Ryu, J.-C. Shin, A. Sahasrabudhe, K. S. Kim, S.-H. Bae, K. Kang, J. Kim, S. Oh, J.-H. Park, *Adv. Mater.* **2025**, 2418582.
[39] F. Liu, S. Zheng, X. He, A. Chaturvedi, J. He, W. L. Chow, T. R. Mion, X. Wang, J. Zhou, Q. Fu, H. J. Fan, B. K. Tay, L. Song, R.-H. He, C. Kloc, P. M. Ajayan, Z. Liu, *Adv. Funct. Mater.* **2016**, *26*, 1169.
[40] W. Zhao, Z. Ghorannevis, K. K. Amara, J. R. Pang, M. Toh, X. Zhang, C. Kloc, P. H. Tan, G. Eda, *Nanoscale* **2013**, *5*, 9677.
[41] M. Karim, J. M. Joao, M. Ramsteiner, *J. Raman Spectrosc.* **2020**, *51*, 2468.
[42] Y. Liao, K. Tu, X. Han, L. Hu, J. W. Connell, Z. Chen, Y. Lin, *Sci. Rep.* **2015**, *5*, 14510.
[43] A. Varghese, D. Saha, K. Thakar, V. Jindal, S. Ghosh, N. V. Medhekar, S. Ghosh, S. Lodha, *Nano Lett.* **2020**, *20*, 1707.
[44] G. H. Yousefi, *Mater. Lett.* **1989**, *9*, 38.
[45] C. Wang, S. Yang, W. Xiong, C. Xia, H. Cai, B. Chen, X. Wang, X. Zhang, Z. Wei, S. Tongay, J. Li, Q. Liu, *Phys. Chem. Chem. Phys.* **2016**, *18*, 27750.
[46] J. Shim, S. Oh, D.-H. Kang, S.-H. Jo, M. H. Ali, W.-Y. Choi, K. Heo, J. Jeon, S. Lee, M. Kim, Y. J. Song, J.-H. Park, *Nat. Commun.* **2016**, *7*, 13413.
[47] M. Sun, Q. Fang, D. Xie, Y. Sun, L. Qian, J. Xu, P. Xiao, C. Teng, W. Li, T. Ren, Y. Zhang, *Nano Res.* **2018**, *11*, 3233.
[48] K. Xu, H. X. Deng, Z. Wang, Y. Huang, F. Wang, S. S. Li, J. W. Luo, J. He, *Nanoscale* **2015**, *7*, 15757.
[49] S. Seo, S. H. Jo, S. Kim, J. Shim, S. Oh, J. H. Kim, K. Heo, J. W. Choi, C. Choi, S. Oh, D. Kuzum, H.-S. Philip Wong, J.-H. Park, *Nat. Commun.* **2018**, *9*, 5106.
[50] S. Yu, *Proc. IEEE* **2018**, *106*, 260.
[51] R. A. John, J. Acharya, C. Zhu, A. Surendran, S. K. Bose, A. Chaturvedi, N. Tiwari, Y. Gao, Y. He, K. K. Zhang, M. Xu, W. L. Leong, Z. Liu, A. Basu, N. Mathews, *Nat. Commun.* **2020**, *11*, 3211.
[52] S. Seo, J. J. Lee, R. G. Lee, T. H. Kim, S. Park, S. Jung, H.-K. Lee, M. Andreev, K.-B. Lee, K.-S. Jung, S. Oh, H.-J. Lee, K. S. Kim, G. Y. Yeom, Y.-H. Kim, J.-H. Park, *Adv. Mater.* **2021**, *33*, 2102980.
[53] Q. Yang, Z. D. Luo, D. Zhang, M. Zhang, X. Gan, J. Seidel, Y. Liu, Y. Hao, G. Han, *Adv. Funct. Mater.* **2022**, *32*, 202207290.
[54] B. Das, S. Baek, J. Niu, C. Jang, Y. Lee, S. Lee, *ACS Nano* **2023**, *17*, 21297.
[55] P. Wang, J. Li, W. Xue, W. Ci, F. Jiang, L. Shi, F. Zhou, P. Zhou, X. Xu, *Adv. Sci.* **2024**, *11*, 2305679.
[56] J. Bai, D. He, B. Dang, K. Liu, Z. Yang, J. Wang, X. Zhang, Y. Wang, Y. Tao, Y. Yang, *Adv. Mater.* **2024**, *36*, 2401060.
[57] Y. Zhou, J. Fu, Z. Chen, F. Zhuge, Y. Wang, J. Yan, S. Ma, L. Xu, H. Yuan, M. Chan, X. Miao, Y. He, Y. Chai, *Nat. Electron.* **2023**, *6*, 870.
[58] G. Wu, X. Zhang, G. Feng, J. Wang, K. Zhou, J. Zeng, D. Dong, F. Zhu, C. Yang, X. Zhao, D. Gong, M. Zhang, B. Tian, C. Duan, Q. Liu, J. Wang, J. Chu, M. Liu, *Nat. Mater.* **2023**, *22*, 1499.
[59] W. Maass, *Neural. Comput.* **2000**, *12*, 2519.
[60] L. Pi, P. Wang, S. Liang, P. Luo, H. Wang, D. Li, Z. Li, P. Chen, X. Zhou, F. Miao, T. Zhai, *Nat. Electron.* **2022**, *5*, 248.
[61] J. Hur, B. C. Jang, J. Park, D.-I. Moon, H. Bae, J.-Y. Park, G.-H. Kim, S.-B. Jeon, M. Seo, S. Kim, S.-Y. Choi, Y.-K. Choi, *Adv. Funct. Mater.* **2018**, *28*, 1804844.