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Enabling the Angstrom Era: 2D material-based multi-bridge-channel complementary field effect transistors



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This review presents a strategic roadmap for integrating two-dimensional materials (2DMs) into multi-bridge channel (MBC) complementary field-effect transistors (CFETs). It highlights key integration challenges, essential design considerations, and industrialization strategies for 2DM-MBC CFETs. These advances are expected to enable ultra-small, energy-efficient, and high-performance devices in the Angstrom Era that transcend the scaling limitations of silicon technology, paving the way for innovative applications in artificial intelligence (AI), the Internet of Things (IoT), and edge computing.

The artificial intelligence (AI) era has catalyzed a paradigm shift from standalone devices in personal computer (PCs) and smartphones to human-centric hyper-connected environments, including smart homes and autonomous vehicles. This transformation generates vast amounts of data, driving continued growth and innovation within the semiconductor industry while creating an unprecedented demand for high-speed, high-density, energy-efficient, and cost-effective devices. Historically, the industry has adapted to this demand by scaling up silicon (Si) wafer sizes—from 100 mm in the 1970s to 300 mm in the 2000s—and through continuous advancements in the miniaturization of Si-based devices¹.

However, as technology nodes approach sub-3 nm dimensions, intrinsic limitations of silicon channels in logic transistors pose substantial challenges to further device scaling^{2,3}. Rather than focusing solely on miniaturization, the industry is shifting towards three-dimensional (3D) device stacking. This strategy that leverages both the 2D surface area and 3D volumetric space of wafers to achieve higher integration density while minimizing device size. Despite the potential of this approach, unexpected issues related to 3D integration persist, underscoring the need for innovative architecture-designs and component-materials to overcome these limitations and enable compact, efficient, and stable 3D device architectures (Fig. 1).

Two-dimensional materials (2DMs), defined by their angstrom-scale thickness, stable surface properties, unique electronic structures, and superior thermal properties, are promising candidates for advanced logic transistors at sub-1 nm technology nodes, referred to as the angstrom era⁴. These materials offer high carrier mobility, mitigate short-channel effects,

and support gate length scaling—key requirements for next-generation devices^{3,5–12}. The thin-channel body structure also facilitates a reduction in standard cell height (z-direction), which not only reduces power consumption but also supports higher device density through multiple-tier stacking. Over the past decade, significant advances have been made in the large-area growth of 2DMs¹³, reduction of contact resistance¹⁴, control of equivalent oxide thickness (EOT)¹⁵, and reduction of middle-of-line (MOL) parasitic capacitance¹⁶. Despite these achievements, the semiconductor industry has historically been conservative in adopting new materials, especially in the intricate architectures of logic transistors.

However, very encouragingly, the 2022 International Roadmap for Devices and Systems (IRDS)—a strategic guide by leading semiconductor manufacturers—acknowledges the need for 2DM integration in 3D devices, particularly at the 0.7 nm technology node (2034 year), marking the dawn of the “Angstrom Era” (Fig. 1 left)¹⁷. This pivotal moment calls for a decisive advancement in the design and integration of sophisticated 3D device architectures. Specifically, the development of 3D stacking channels, such as 2DM-based multi-bridge-channel (2DM-MBC) and 3D stacking (3DS) devices, complementary field-effect transistor (CFET, aka 3DS-FET) architectures¹⁸, as well as interconnect innovations grounded in Design Technology Co-Optimization (DTCO) and System Technology Co-Optimization (STCO), is essential to overcoming current barriers and driving transformative progress in semiconductor technology^{19,20} (Fig. 1 right). However, significant progress is still needed, as effective control over 3D device architectures remains an unresolved challenge.

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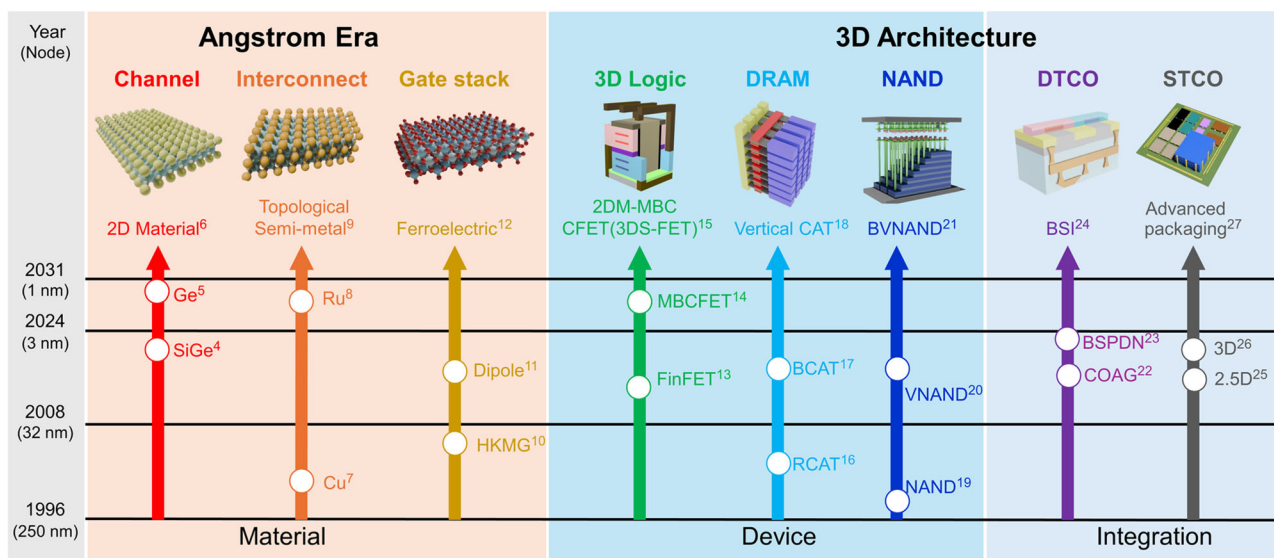


Fig. 1 | Development history and future direction of semiconductor device technology: material, device and integration. This figure outlines the progression of semiconductor technology, categorized into three main areas: materials, devices, and integration strategies. The Angstrom era highlights advancements in channel materials (2D materials), interconnects (topological semimetals), and gate stacks (ferroelectric materials) as devices approach sub-1 nm nodes. On the device side,

innovations such as 2DM-MBC and CFET logic, along with vertical channel structures for DRAM and NAND, exemplify the move towards 3D architectures. Integration methodologies like DTCO and STCO, including advanced packaging and back-side power delivery, are essential to realizing compact, high-performance 3D architectures^{5,17,76–98}.

This review article provides a critical and comprehensive examination of integration strategies for 2DMs in advancing 3D logic-integrated architectures, with a specific focus on CFETs. It begins by discussing design directions and key considerations for CFET structures (Session I, Fig. 2). Following this, it explores Si-based MBC CFET processes (Session II, Fig. 3) and examines current advancements, challenges, and innovation pathways for integrating 2DM-based MBC CFET structures (Session III, Fig. 4). Finally, it addresses the performance requirements for industrialization, focusing on the challenges of scaling up for reliable and robust industrial applications (Session IV, Fig. 5). By synthesizing the current state of research and development in 2DMs and 3D integration technologies, this review aims to provide a detailed roadmap for future advancements in the field. It highlights the importance of continued innovation and collaboration between academia and industry to overcome existing barriers and realize the full potential of next-generation semiconductor devices.

Integration process of Si-MBC FETs and challenges in transitioning to 2DM-MBC FETs

The gate-all-around (GAA) architecture in FETs provides significant advantages in electrical performance, including enhanced gate control, reduced leakage current, lower operating voltage for improved power efficiency, and minimized short-channel effects (SCE)²¹. Furthermore, the MBC structure, compared to conventional GAA, provides a relatively wider effective channel width, resulting in higher saturation current and superior scalability, making it highly suitable for high-performance applications²². These advantages make the MBC configuration a foundational element for the CFET architecture. However, several key challenges remain in the MBC integration process when using 2DMs, which is why recent implementations of CFETs with 2DMs have primarily focused on 2D planar FETs rather than 2D-MBC FETs^{5,10–12}. This session, as illustrated in Fig. 2, outlines the key requirements for integrating 2DMs into the MBC FET structure and proposes potential solutions and future directions to overcome these challenges while accommodating the unique properties of 2DMs.

- (i) **Large-area, high-quality 2DMs epitaxial growth:** In Si-MBC FETs, the epitaxial growth of Si/SiGe stacks is a well-established and reliable process that consistently produces defect-free layers over large areas.

However, achieving large-area, high-quality growth of 2DM channels, such as MoS₂ and WSe₂, remains challenging due to their sensitivity to processing conditions, including temperature, humidity, and pressure. Current chemical vapor deposition (CVD) techniques often result in small grain sizes and numerous defects, which negatively impact device performance. To address these challenges, alternative low-temperature methods, such as plasma-enhanced atomic layer deposition (PE-ALD) and molecular beam epitaxy (MBE), are being investigated to facilitate the wafer-scale growth of high-quality, single-crystalline 2DMs with uniform properties and minimal defects^{12,23}.

- (ii) **Stable free-standing structure formation of 2DM channels:** In Si-MBC FET integration, Si channels are released by selectively etching a sacrificial SiGe layer, a relatively straightforward process owing to the mechanical robustness of silicon. However, forming stable, free-standing 2DM channels is far more challenging due to their atomically thin nature. For instance, during the channel release process, the selective etching of dummy gate materials or sacrificial layers can cause considerable damage to 2DM channels. To address this issue, low-power plasma etching techniques are being developed to minimize damage, and post-etch healing processes are employed to restore the crystalline structure of 2DM channels, thereby enhancing their mechanical and electrical properties^{24–26}. Additionally, alternative approaches, such as dry etching and critical-point drying, are being explored to reduce capillary forces and ensure the stability of free-standing 2DM channels²⁷.
- (iii) **Formation of high-quality gate structure surrounding the channel:** Constructing a defect-free, four-sided gate structure around 2DM channels is challenging due to their atomic-scale thickness and extreme sensitivity to surface defects and contamination. Consequently, many studies focused on 2DM-MBC FETs struggle to demonstrate optimal device performance^{9,28}. To address these challenges, high-k dielectrics such as Al₂O₃ and HfO₂ can be deposited using ALD or MBE in ultrahigh vacuum (UHV) environments to achieve defect-free interfaces on the dangling-bond-free surfaces of 2DMs^{7,18,29,30}. Techniques such as plasma surface activation, contamination removal, and post-deposition annealing are critical for maintaining interface stability and preventing contamination. Furthermore, the

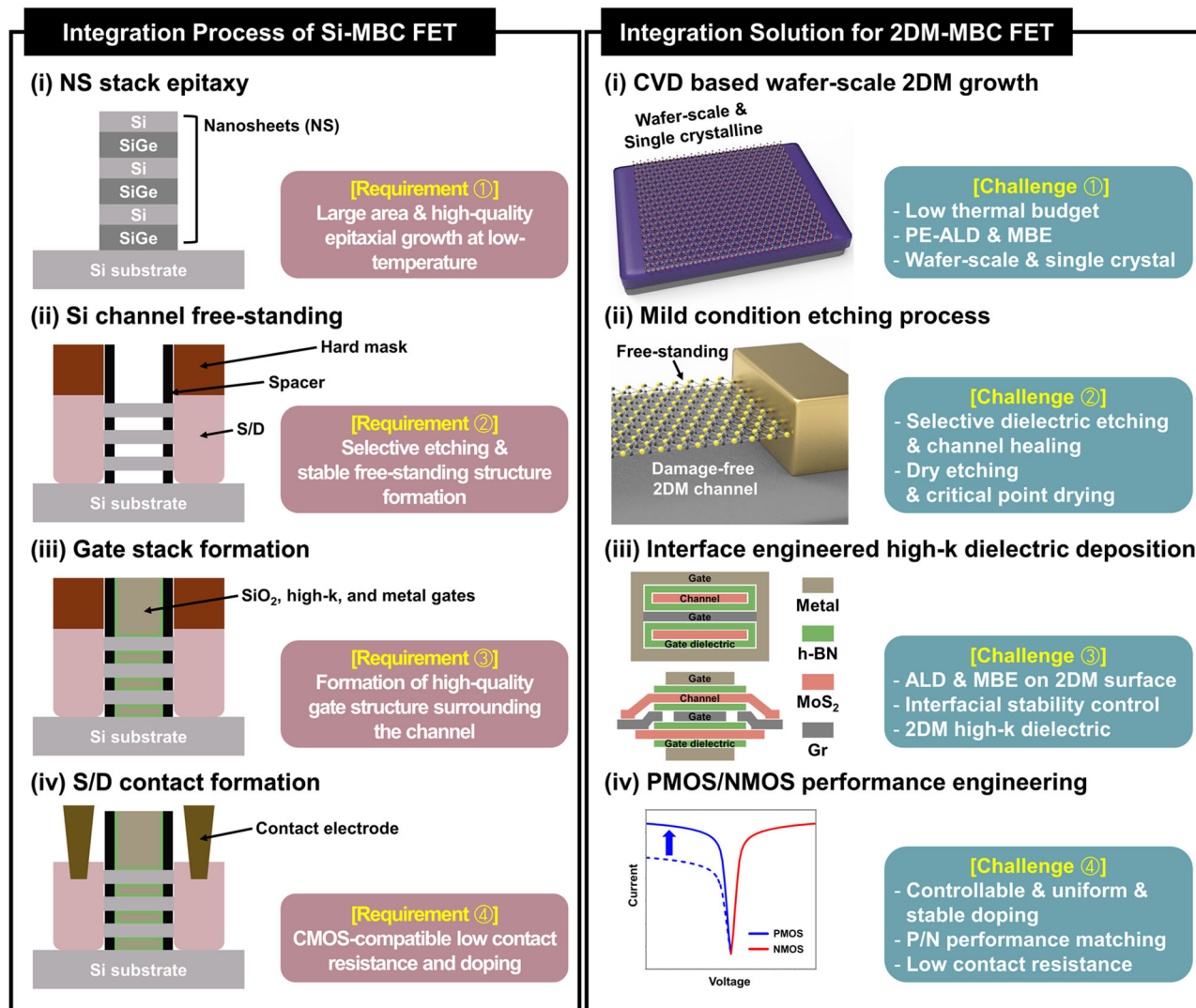


Fig. 2 | Integration process of Si-MBC FETs and transition challenges for 2DM-MBC FETs. The left panel illustrates the requirements of conventional integration process for Si-based MBC FETs, which includes four main steps: (i) large-area and high-quality epitaxial growth of Si/SiGe stacks, (ii) selective etching to create stable, free-standing Si channels, (iii) formation of a high-quality gate structure surrounding the channel, and (iv) low-resistance source/drain contacts and doping compatible with CMOS. The right panel highlights the specific challenges of adapting this process for 2DM-based MBC FETs and proposes potential solutions.

Key challenges in adapting Si process to 2DMs are highlighted: (i) achieving wafer-scale, single crystalline epitaxial growth of 2DMs at low temperature, (ii) maintaining stable free-standing and damage-free 2DM channels during the release process, (iii) depositing high-k dielectrics on 2DM surfaces and controlling interfacial stability, and (iv) developing CMOS-compatible doping and low contact resistance techniques for 2DMs. The right panel outlines potential solutions to these challenges.

development of high-k dielectric 2DMs could further stabilize the interface with 2DM channels, ensuring long-term device reliability^{31,32}.

- (iv) **CMOS-compatible low contact resistance and doping:** In Si MBCFETs, traditional doping techniques, such as ion implantation, are commonly used to control the electrical properties of the channel and minimize contact resistance. However, these approaches are unsuitable for 2DMs, as they can cause significant damage to the atomically thin 2D layers. Therefore, the development of damage-free doping methods for 2DMs is crucial for achieving low contact resistance and high device performance. Substitutional doping techniques, such as Nb-doped MoS₂ and V-doped WSe₂, have demonstrated potential in modulating the electrical properties of 2DMs without causing substantial damage^{33,34}. Additionally, gate stack-induced permanent channel doping offers precise control over doping levels while preserving the structural integrity of the 2DM channel^{35–37}. Reducing contact resistance between 2DMs and metal

electrodes remains another critical challenge. This issue can be alleviated by incorporating semi-metals like Bi and Sb, doping the contact region of 2DM channels, or exploring naturally P-type materials such as Te and TeO₂ to enhance PMOS performance^{38–44}.

Design directions and key considerations for CFET structures

Building on the foundational advances of 2DM-MBC FETs, CFETs are gaining attention for their potential to offer significant improvements in Performance, Power, Area, and Cost (PPAC). CFETs represent a next-generation architecture that addresses many of the limitations of conventional transistor designs by stacking PMOS and NMOS devices in a three-dimensional configuration. This architectural innovation provides promising pathways for continued scaling beyond the limits of traditional planar transistors. As shown in Fig. 3, to achieve optimal outcomes in CFET structures, three main key factors in 3D device architecture must be carefully considered: (i)

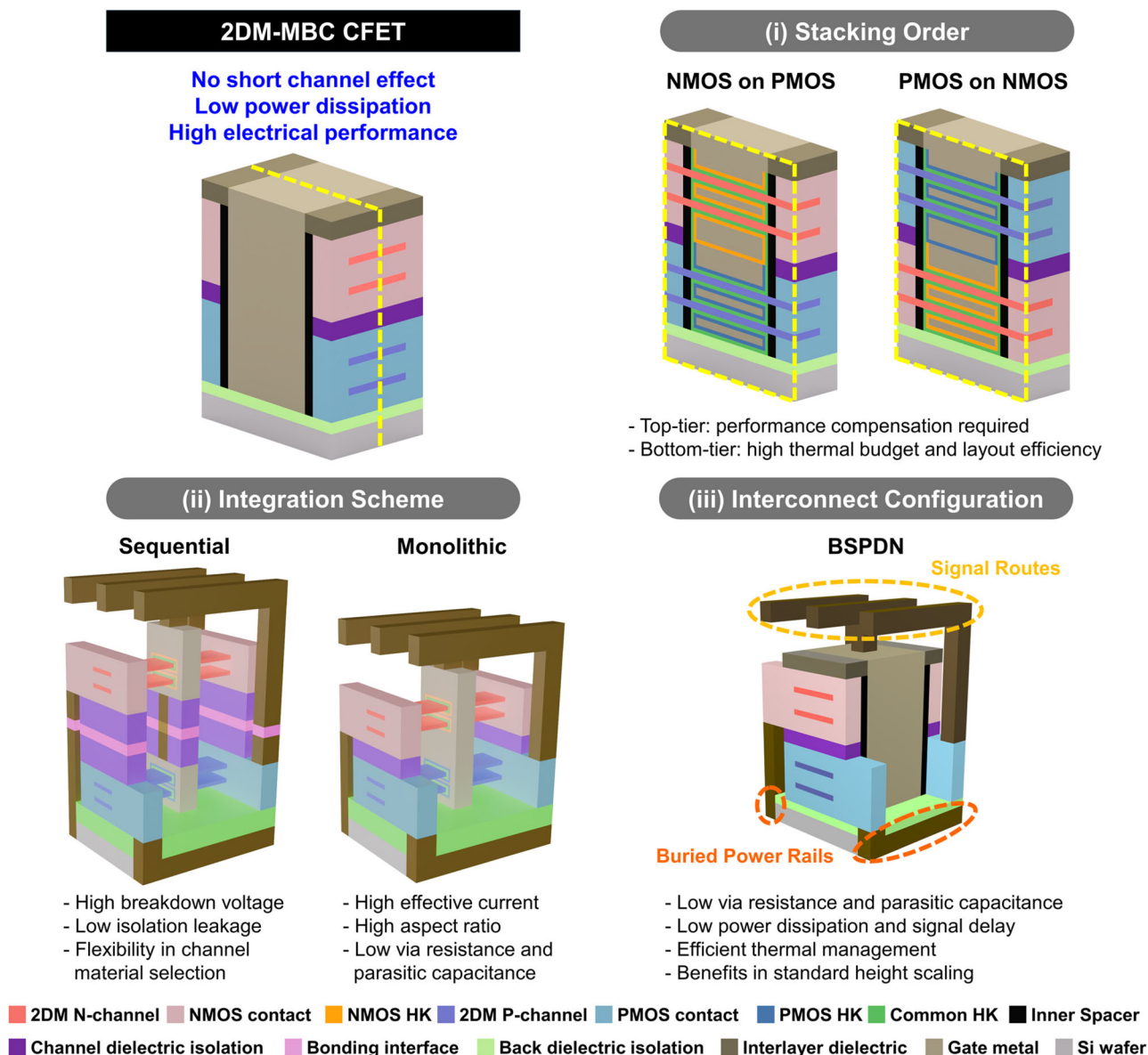


Fig. 3 | Structural Overview of 2DM-MBC CFETs and Key Design Considerations for Optimal Performance. The diagram is divided into three main factors in 3D device architecture: (i) stacking order, (ii) integration scheme, and (iii)

interconnect configuration. Each section represents critical parameters to enhance electrical performance, layout efficiency, process simplification, cost efficiency, and reliability.

the stacking order of P-Channel Metal-Oxide-Semiconductor (PMOS) and N-Channel Metal-Oxide-Semiconductor (NMOS); (ii) stacking integration, including sequential versus monolithic; and (iii) the interconnect configuration, particularly the power delivery network (PDN)^{23–27}.

- (i) **Stacking order:** In CFETs, the MBC structure is utilized in both NMOS and PMOS structures to improve device performance, as discussed in Session I. The stacking order plays a critical role in determining overall performance and process compatibility, influenced by the characteristics and thermal requirements of each layer. The bottom layer is designed to accommodate high-temperature processes, providing a higher thermal budget and enabling a simplified layout. In contrast, the top layer is constrained by lower process temperatures and stricter layout considerations to prevent degradation of the bottom layer's performance or stability. For instance, deposition, annealing, and implantation processes for the top layer must achieve equivalent performance metrics, such as mobility and on-current, under mild processing conditions to match the bottom channel^{23,24}. Thus, the P/

NMOS ordering is crucial for optimizing CFET performance, ensuring CMOS equivalence, and maintaining compatibility with advanced integration processes.

- (ii) **Integration Scheme:** CFETs can be integrated using either sequential or monolithic stacking, each offering distinct advantages. Sequential CFETs involve bonding two separate wafers, one containing NMOS and the other containing PMOS FETs. This approach provides flexibility in material selection and integration environments. The larger separation between channel dielectrics results in higher breakdown voltage and lower leakage current. However, the wafer bonding process increases device height and effective interconnect pitch, leading to higher parasitic capacitance and resistance, which in turn elevate power consumption and induce signal delay. Additionally, sequential integration is highly sensitive to misalignment and limited by the thermal budget. In contrast, monolithic CFETs are directly integrated on a single wafer by aligning top- and bottom-tier devices, making them cost-effective and suitable for height scaling^{5,10,25}. This configuration reduces parasitic capacitance and resistance, enabling higher effective

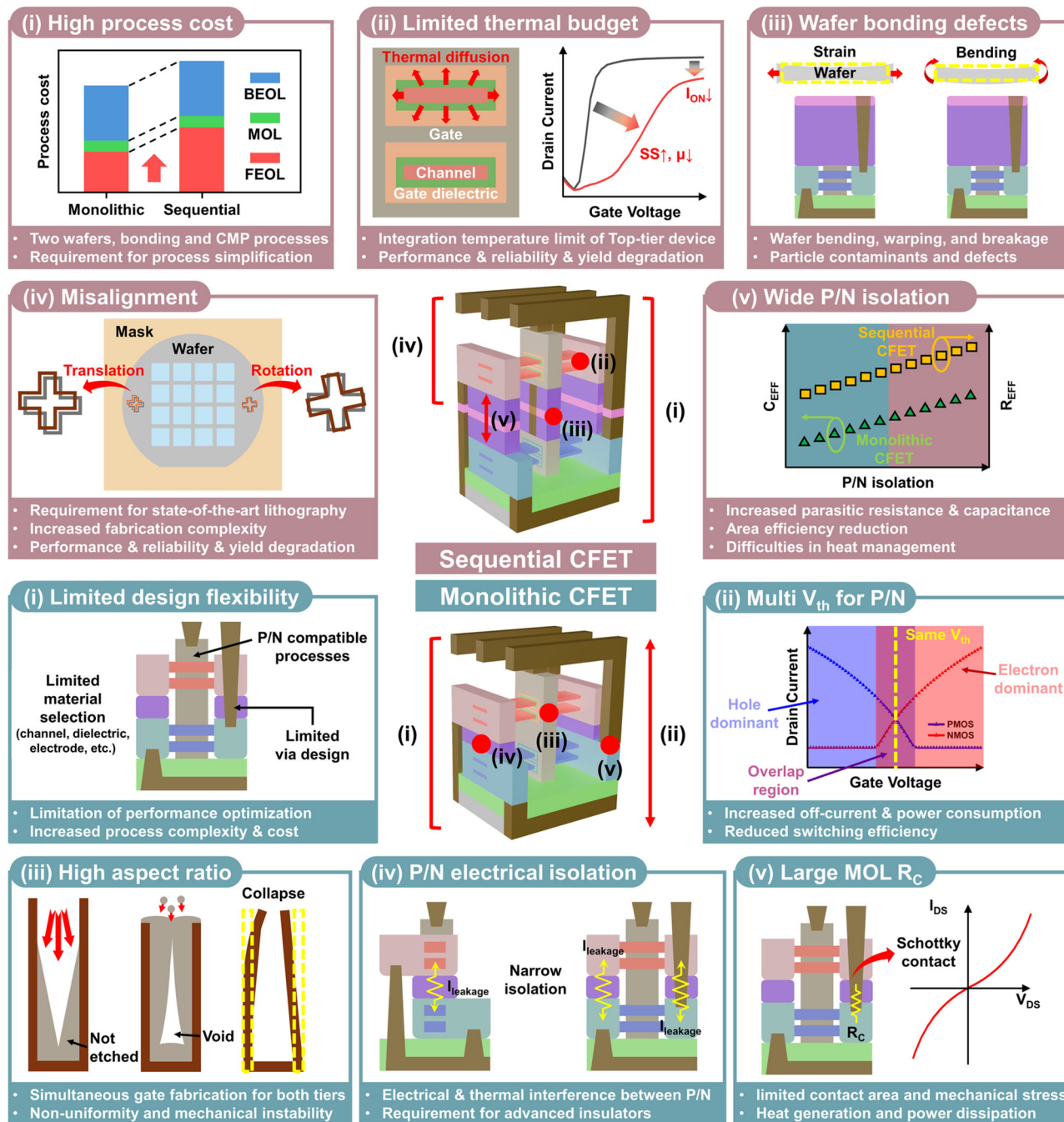


Fig. 4 | Integration challenges of sequential and monolithic CFET architectures. Technical challenges are addressed in device performance, thermal management, process integration, and manufacturing complexity for both architectures. The top panel depicts the challenges associated with sequential CFETs, including (i) high process costs, (ii) limited thermal budget, (iii) wafer bonding defects, (iv) misalignment between top-tier and bottom-tier devices, and (v) wide isolation between

P and N devices. The lower panel shows the challenges of monolithic CFETs, which include (i) limited design flexibility, (ii) difficulty in separating threshold voltages for P and N transistors, (iii) high aspect ratio structures, (iv) challenges in ensuring electrical isolation between P and N devices, and (v) increased contact resistance in bottom devices.

current generation, i.e., lower power consumption. However, it introduces design complexity and poses reliability challenges due to the narrow dielectric isolation between P/NMOS channels. Further integration challenges associated with sequential and monolithic 3D FETs will be explored in Session III.

- (iii) **Interconnect Configuration:** While interconnection layers constantly increase (more than 13 layers in back-end-of-line (BEOL)) to connect already scaled-down FETs, the interconnect configuration becomes more serious in 3D device architecture. The back-side power delivery

network (BSPDN) offers a promising solution by positioning logic circuits on the front side and power supply or signal routing on the back side, thereby improving power efficiency over conventional interconnects. This arrangement enables broader and more direct pathways, minimizing the resistance and capacitance of metal interconnects and avoiding the complexity of the BEOL stack. This improvement enhances efficiency for front-end routing, signal integrity, and timing accuracy. Overall, BSPDN alleviates routing congestion and supports further reductions in standard cell height,

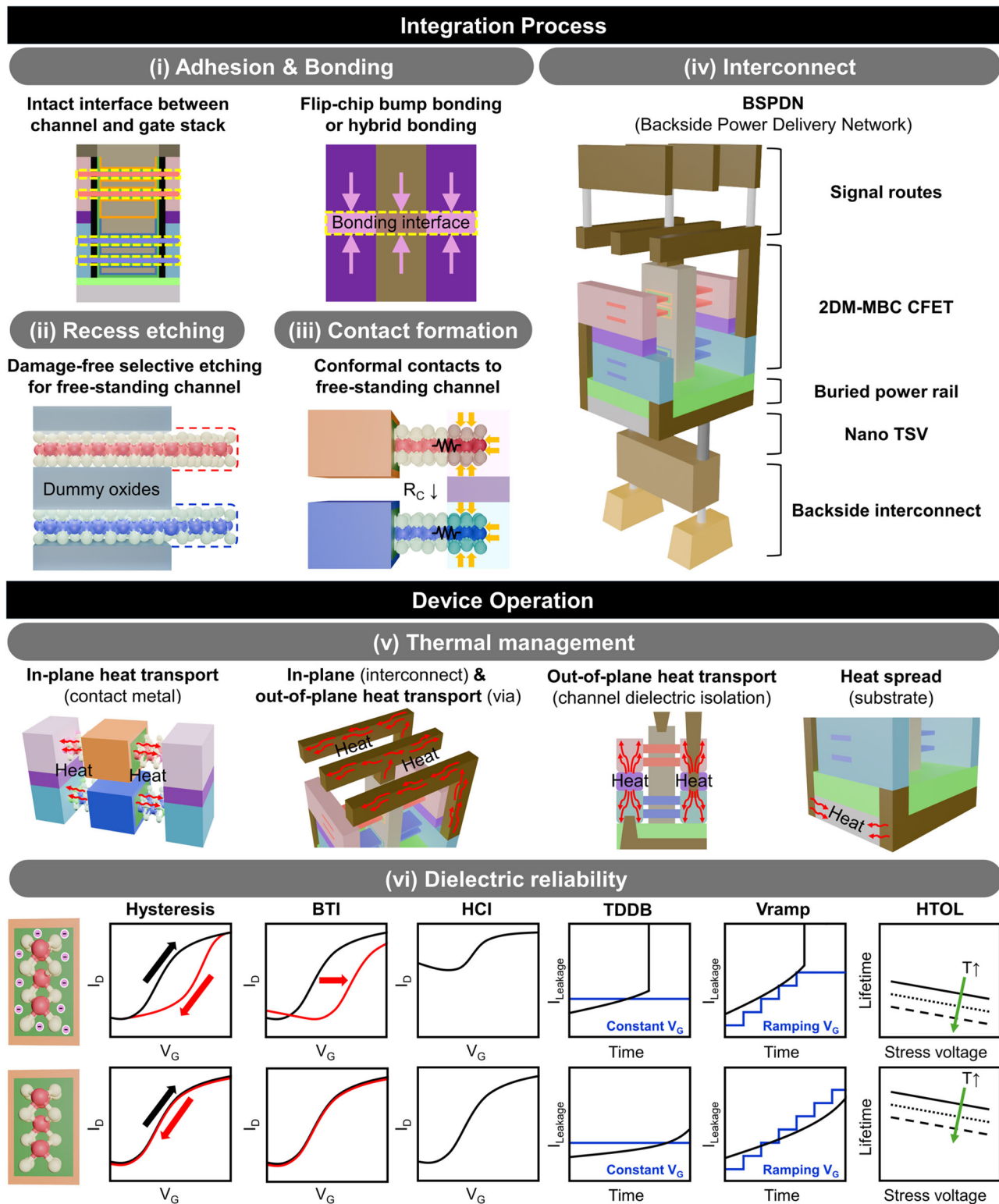


Fig. 5 | Reliability considerations for process integration and device operation of 2DM-MBC CFETs. Key challenges in integration process include (i) adhesion and bonding, (ii) recess etching, (iii) contact formation, and (iv) interconnect and power

management. Critical considerations for device operation include (v) thermal management and (vi) dielectric reliability.

which is crucial for 3D architectures, where stacking increases the vertical interconnect pitch and facilitates semiconductor chip miniaturization^{26,27}. Requirements for 2DM-MBC CFET reliability, including interconnect configurations, will be further discussed in Session IV.

Integration challenges of sequential and monolithic CFETs

CFETs introduce a set of unique challenges that must be addressed to realize their advantages fully. This session discusses the key integration difficulties associated with the two primary CFET architectures:

Table 1 | Integration challenges of sequential and monolithic CFET

Integration scheme	Sequential CFET	Monolithic CFET
Process cost	High	Low
Thermal budget	Limited	Limited
Bonding defect	Many	Few
Alignment	Misalign	Precise align
P/N isolation	Wide	Narrow
Design flexibility	Unlimited	Limited
Multi V_{th}	Straightforward	Complicated
Aspect ratio	Low	High
Electrical isolation	Good	Poor
MOL R_C	Small	Large

sequential CFETs and monolithic CFETs. Each architecture presents distinct technical challenges in terms of device performance, thermal management, process integration, and manufacturing complexity, as summarized in Fig. 4 and Table 1.

Challenges in sequential CFETs

Sequential CFETs involve fabricating the bottom-tier device first, followed by wafer bonding with a top-tier wafer that contains only the pre-formed channel. The top-tier device is then integrated sequentially through chemical-mechanical polishing (CMP) and BEOL processes. This approach offers greater flexibility in material selection and processing, as each device layer can be independently optimized before integration. However, this flexibility also introduces several critical challenges:

- (i) **High process cost:** The use of two wafers, along with bonding and CMP steps, significantly increases manufacturing costs. Additionally, the increased wafer thickness extends interconnect length, further complicating integration and raising fabrication expenses. Process simplification and cost-reduction strategies are essential for enabling commercial scalability^{45,46}.
- (ii) **Limited thermal budget:** Fabrication of the top-tier device requires a series of advanced lithography steps and low-temperature processing to prevent degradation of the bottom-tier device^{47,48}. Issues such as dopant diffusion and gate dielectric instability can degrade carrier transport properties^{49,50}. While plasma-assisted deposition and other low-temperature techniques help mitigate these risks, they introduce further process complexity.
- (iii) **Wafer bonding defects:** Wafer bonding integrates top-tier devices on bottom-tier wafers but can cause mechanical stress, leading to warping, bending, or breakage, which affects yield and reliability. Additionally, contaminants or defects at the bonding interface can also impact performance. Advanced bonding techniques with improved defect control are crucial for overcoming these issues.
- (iv) **Misalignment:** Precise alignment between the top-tier and bottom-tier devices is critical in sequential CFETs to avoid performance degradation⁵¹. Misalignment can increase parasitic resistance and capacitance, negatively impacting device speed and power consumption. The requirement for advanced lithography tools, such as extreme ultraviolet (EUV), to achieve this precision further adds to the cost and complexity of manufacturing.
- (v) **Wide P/N isolation:** Sequential CFETs require wide isolation between the PMOS and NMOS devices to prevent crosstalk and ensure proper operation. However, this wide isolation increases thermal resistance and parasitic capacitance or resistance, which can degrade overall device performance^{45,52}. Moreover, the increased area required for isolation reduces the density of devices, which is counterproductive to scaling goals⁴⁶.

Challenges in monolithic CFETs

Monolithic CFETs integrate both top- and bottom-tier devices on a single wafer, forming the channels first, followed by source/drain and gate formation, inter-tier middle-of-line (MOL) connections, and BEOL processing. This compact approach eliminates wafer bonding and minimizes alignment errors but introduces its own challenges:

- (i) **Limited design flexibility:** Monolithic CFETs require simultaneous fabrication of PMOS and NMOS devices, restricting their independent optimization^{46,53}. Finding materials and processes that meet the distinct requirements of both device types is a significant challenge. This lack of flexibility complicates process integration and limits performance optimization.
- (ii) **Multi V_{th} for P/N devices:** Achieving separate threshold voltages (V_{th}) for the PMOS and NMOS devices is critical for optimal switching behavior^{54–56}. However, the shared processing environment complicates doping and gate stack engineering, leading to increased leakage and power consumption. Advanced doping techniques are needed to ensure precise V_{th} control.
- (iii) **High aspect ratio:** The tall and narrow structures required for monolithic CFETs create challenges in etching, deposition, and patterning. Simultaneous gate fabrication for both tiers necessitate high aspect ratio processing, making these structures prone to non-uniformity and mechanical instability, increasing defect risks. Additionally, the increased complexity of these structures can result in longer production times and higher manufacturing costs.
- (iv) **P/N electrical isolation:** Ensuring effective electrical and thermal isolation between the PMOS and NMOS devices is critical in monolithic CFETs to prevent leakage currents and thermal interference^{57,58}. Poor isolation can lead to increased crosstalk, elevated leakage, and reduced device reliability. Advanced insulators and optimized isolation techniques are essential for maintaining electrical and thermal separation, thereby overcoming this challenge.
- (v) **Large middle-of-line R_C :** The bottom-tier devices in Monolithic CFETs experience increased contact resistance due to limited contact area and mechanical stress from the top-tier devices^{59–61}. This increased resistance degrades the performance of the bottom-tier devices, leading to higher power dissipation and heat generation. Solutions such as utilizing semi-metals or advanced contact engineering are necessary to minimize R_C and enhance the overall reliability and performance of Monolithic CFETs.

Currently, Si-based sequential CFETs are an ongoing process development. The implementation of sequential and monolithic CFETs using 2DM-MBC has more hurdles. However, to achieve the ultimate goal of compact 2DM-MBC-based monolithic CFETs, it is crucial not only to refine fabrication processes innovatively but also to creatively advance materials, such as 2D channels, metals, and low-k dielectrics, that retain stability under aggressive scaling conditions.

Promising integration strategies for enhancing the reliability of 2DM-MBC CFETs

This section examines key factors that must be addressed to ensure the reliability of both the integration process and device operation of 2DM-MBC CFETs, thereby facilitating the transition from laboratory innovations to high-volume manufacturing.

- (i) **Adhesion and Bonding:** Adhesion properties crucial for achieving high fabrication yields and device reliability, particularly during high-temperature processing or under mechanical strain. Specifically, the inert nature of 2DM surfaces affects interfacial adhesion with surrounding materials, which impacts integration efficiency and electrical performance. For instance, a robust adhesion between the channel and gate stacks is essential to maintaining device integrity. In monolithic 2DM-MBC CFETs, differences in adhesion energy between top- and bottom-tier channels arise from material selection, processing steps, polarity control, and deposition conditions. When a

- common gate controls both PMOS and NMOS devices, these variations can induce mechanical stress, compromising reliability. In sequential 2DM-MBC CFETs, precise control of adhesion energy is necessary for bonding techniques such as flip-chip or hybrid Cu-Cu bonding to ensure high yield and uniformity during top- and bottom-tier integration^{5,6}. Optimized interface engineering and process refinement are critical to achieving reliable and scalable 2DM-MBC CFETs integration.
- (ii) **Recess Etching:** The recess etching process, which is crucial for creating a free-standing 2DM channel, poses challenges, as it may damage the channel material. High-selectivity sacrificial layers are thus vital for ensuring clean etch profiles and preventing damage⁶. Since the free-standing channels formed through recess etching are susceptible to capillary forces during solution-based processes, it is critical to develop etching techniques that minimize such damage. Current research on etching for 2DM focuses on achieving layer-by-layer etching without damage. The KOH etching can be utilized in the recess channel process, demonstrating high etching selectivity for the WO_x/WSe_2 channel and realizing damage-free channels⁶². To form a free-standing 2DM channel that enables conformal contact, techniques that enable all-sided etching of channels are required, employing a sacrificial layer with high etch selectivity.
 - (iii) **Contact Formation:** The formation of low-resistance contact between the 2DM channel and the metal electrode remains challenging^{63–65}. While high doping locally to contact regions is often used to reduce contact resistance, the situation is more complex for 2DMs due to their sensitivity to process-induced crystal defects. Conformal contacts, which form electrical connections on the top, bottom, and edges of the channel, effectively reduce the contact length while increasing the overall contact area. This enables a smaller contacted poly pitch (CPP) while minimizing contact resistance, a critical requirement for efficient 3D integration⁶. While edge contacts have received considerable attention^{14,66,67}, further research into conformal contact approaches, incorporating factors such as CMOS-compatible metal deposition and high thermal budget, is needed to fully optimize contact resistance^{4,63–65}.
 - (iv) **Interconnect:** The BSPDN, which places the power delivery network on the wafer's backside, plays a crucial role in interconnect design by reducing voltage drop, enhancing power efficiency, minimizing footprint, and improving overall performance⁶⁵. Key technologies such as buried power rail (BPR), which embeds power rails within the Si substrate, and nano through-silicon vias (nano-TSVs) through silicon enable sub-micron interconnect pitch^{68,69}. However, BSPDN integration for 2DM-MBC FETs is still in its early stages, and significant technical challenges are expected for its integration into 2DM-MBC CFETs¹⁶.
 - (v) **Thermal Management:** A densely packed 3D architecture like MBC CFET requires effective thermal management, as increased power density can create localized hotspots, degrading performance and reliability⁷⁰. Thermal transport in 2DMs has been extensively studied for thermal management in the 3D integration of 2DM FETs^{65,71}. Heat dissipation strategies include device structure engineering, such as backside power delivery (BPR) engineering to reduce thermal resistance and enhance drive current, and material property engineering, which mitigates self-heating through defect control⁷², heterostructures⁷³, doping⁷⁴, and strain⁷⁵. Further research into in-plane and out-of-plane heat transport across contacts, interconnects, vias, and dielectric isolation is essential for optimizing thermal management in 2DM-MBC CFETs.
 - (vi) **Dielectric Reliability:** Ensuring device reliability is critical for the qualification of 2DM-MBC CFETs, particularly in addressing defects and charge trapping in the dielectric. Process integration must minimize dangling bonds in the 3D dielectric oxides and strain-induced defects in the gate stacks, which can lead to charge trapping at interfaces and border traps. However, these factors are often overlooked in academic studies. Key reliability tests include hysteresis

and bias temperature instability (BTI) monitored by V_{th} shift, hot carrier injection (HCI) evaluated by gate-induced drain leakage (GIDL), time-dependent dielectric breakdown (TDDB) assessed via breakdown voltage or voltage ramping (V_{ramp}), and high-temperature operating lifetime (HTOL) testing. Selecting dielectrics optimized for 2DM channels and ensuring thorough monitoring of these reliability metrics in 3D-integrated structures are essential. Identifying optimal materials and advancing process integration within a comprehensive reliability framework must be addressed to realize the full potential of 2DM-MBC CFETs for next-generation logic transistors^{4,63–65}.

Conclusion and outlook

The development of 2DM-MBC FET and CFET architectures is still in its early stages, with many challenges yet to be fully addressed. However, this paper provides a comprehensive analysis of the advantages, critical challenges, and key development strategies along with potential improvement paths that are expected to accelerate the advancement of this field. If successfully implemented, the 2DM-MBC CFET will revolutionize semiconductor technology, enabling ultra-small, high-performance, and energy-efficient devices that surpass the limitations of current silicon-based architectures. This advancement will not only enhance computing performance and efficiency but also fundamentally transform the technological landscape by opening the door to new applications in the IoT, AI, and edge computing, bringing us closer to the era of ubiquitous intelligent connectivity.

Data availability

No datasets were generated or analysed during the current study.

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References

- Waldrop, M. M. The chips are down for Moore's law. *Nature* **530**, 144 (2016).
- Uchida, K. et al. Experimental study on carrier transport mechanism in ultrathin-body SOI nand p-MOSFETs with SOI thickness less than 5 nm. in *Proc. International Electron Devices Meeting (IEDM)*, 47–50, (IEEE, 2002).
- Liu, C. et al. Two-dimensional materials for next-generation computing technologies. *Nat. Nanotechnol.* **15**, 545–557 (2020).
- Zeng, S., Liu, C. & Zhou, P. Transistor engineering based on 2D materials in the post-silicon era. *Nat. Rev. Electr. Eng.* **1**, 335–348 (2024).
- Jayachandran, D., Sakib, N. U. & Das, S. 3D integration of 2D electronics. *Nat. Rev. Electr. Eng.* **1**, 300–316 (2024).
- Kim, K. S. et al. The future of two-dimensional semiconductors beyond Moore's law. *Nat. Nanotechnol.* **19**, 895–906 (2024).
- Huang, X. et al. High drive and low leakage current MBC FET with channel thickness 1.2 nm/0.6 nm. in *Proc. IEEE International Electron Devices Meeting (IEDM)*, 12.1.1–12.1.4 (IEEE, 2020).
- Liu, M. G. et al. Large-scale ultrathin channel nanosheet-stacked CFET based on CVD 1L $\text{MoS}_2/\text{WSe}_2$. *Adv. Electron. Mater.* **9**, 2200722 (2023).
- Huang, X. et al. Ultrathin multibridge channel transistor enabled by van der Waals assembly. *Adv. Mater.* **33**, 2102201 (2021).
- Kang, J. H. et al. Monolithic 3D integration of 2D materials-based electronics towards ultimate edge computing solutions. *Nat. Mater.* **22**, 1470–1477 (2023).
- Kim, J. Y., Ju, X., Ang, K. W. & Chi, D. Z. Van der Waals layer transfer of 2D materials for monolithic 3D electronic system integration: review and outlook. *ACS Nano* **17**, 1831–1844 (2023).
- Lu, K., Shim, J., Kim, K. S., Kim, S. W. & Kim, J. 2D materials can unlock single-crystal-based monolithic 3D integration. *Nat. Electron.* **7**, 416–418 (2024).

13. Seol, M. et al. High-throughput growth of wafer-scale monolayer transition metal dichalcogenide via vertical Ostwald ripening. *Adv. Mater.* **32**, 2003542 (2020).
14. Schulman, D. S., Arnold, A. J. & Das, S. Contact engineering for 2D materials and devices. *Chem. Soc. Rev.* **47**, 3037–3058 (2018).
15. Illarionov, Y. Y. et al. Insulators for 2D nanoelectronics: the gap to bridge. *Nat. Commun.* **11**, 3385 (2020).
16. Kim, J. S. et al. Addressing interconnect challenges for enhanced computing performance. *Science* **386**, eadk6189 (2024).
17. *International Roadmap for Devices and Systems (IRDS™) 2022 Edition*. <https://irds.ieee.org/editions/2022> (IEEE, 2022).
18. Xia, Y. et al. Wafer-scale demonstration of MBC-FET and C-FET arrays based on two-dimensional semiconductors. *Small* **18**, 2107650 (2022).
19. Moroz, V. et al. DTCO launches Moore's law over the feature scaling wall. in *Proc. IEEE International Electron Devices Meeting (IEDM)*, 41.1.1–41.1.4 (IEEE, 2020).
20. Biswas, D., Myers, J., Ryckaert, J. & Samavedam, S. B. STCO: driving the more than Moore era. in *Proc. IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 7–8 (IEEE, 2024).
21. Bae G. et al. 3nm GAA technology featuring multi-bridge-channel FET for low power and high performance applications. in *Proc. IEEE International Electron Devices Meeting (IEDM)*, 28.7.1–28.7.4 (IEEE, 2018).
22. Yoon E. et al. Sub 30 nm multi-bridge-channel MOSFET (MBCFET) with metal gate electrode for ultra high performance application. in *Proc. IEDM Technical Digest. IEEE International Electron Devices Meeting*, 627–630 (IEEE, 2004).
23. Moore, A. L. & Shi, L. Emerging challenges and materials for thermal management of electronics. *Mater. Today* **17**, 163–174 (2014).
24. Song, H. F. et al. Two-dimensional materials for thermal management applications. *Joule* **2**, 442–463 (2018).
25. O'Brien, K. P. et al. Process integration and future outlook of 2D transistors. *Nat. Commun.* **14**, 6400 (2023).
26. Radhakrishnan, K., Swaminathan, M. & Bhattacharyya, B. K. Power delivery for high-performance microprocessors-challenges, solutions, and future trends. *IEEE Trans. Compon., Packag. Manuf. Technol.* **11**, 655–671 (2021).
27. Chen, R. et al. Opportunities of chip power integrity and performance improvement through wafer backside (BS) connection. in *Proc. 24th ACM/IEEE Workshop on System Level Interconnect Pathfinding*, 1–5 (ACM, 2022).
28. Hitesh, S., Dasika, P., Watanabe, K., Taniguchi, T. & Majumdar, K. Integration of 3-level MoS₂ multibridge channel FET with 2D layered contact and gate dielectric. *IEEE Electron Device Lett.* **43**, 1993–1996 (2022).
29. Li, N. et al. Atomic layer deposition of Al₂O₃ directly on 2D materials for high-performance electronics. *Adv. Mater. Interfaces* **6**, 1802055 (2019).
30. Price, K. M. et al. Plasma-enhanced atomic layer deposition of HfO₂ on monolayer, bilayer, and trilayer MoS₂ for the integration of high-κ dielectrics in two-dimensional devices. *ACS Appl. Nano Mater.* **2**, 4085–4094 (2019).
31. Marinov, D. et al. Reactive plasma cleaning and restoration of transition metal dichalcogenide monolayers. *npj 2D Mater. Appl.* **5**, 17 (2021).
32. Lee, S. H. et al. Improvements in structural and optical properties of wafer-scale hexagonal boron nitride film by post-growth annealing. *Sci. Rep.* **9**, 10590 (2019).
33. Suh, J. et al. Reconfiguring crystal and electronic structures of MoS₂ by substitutional doping. *Nat. Commun.* **9**, 199 (2018).
34. Kozhakhmetov, A. et al. Controllable p-Type doping of 2D WSe₂ via vanadium substitution. *Adv. Funct. Mater.* **31**, 2105252 (2021).
35. Rai, A. et al. Air stable doping and intrinsic mobility enhancement in monolayer molybdenum disulfide by amorphous titanium suboxide encapsulation. *Nano Lett.* **15**, 4329–4336 (2015).
36. Alharbi, A. & Shahrjerdi, D. Analyzing the effect of high-κ dielectric-mediated doping on contact resistance in top-gated monolayer MoS₂ transistors. *IEEE Trans. Electron Devices* **65**, 4084–4092 (2018).
37. Ma, J. Y. et al. Top gate engineering of field-effect transistors based on wafer-scale two-dimensional semiconductors. *J. Mater. Sci.* **106**, 243–248 (2022).
38. Shen, P. C. et al. Ultralow contact resistance between semimetal and monolayer semiconductors. *Nature* **593**, 211–217 (2021).
39. Li, W. S. et al. Approaching the quantum limit in two-dimensional semiconductor contacts. *Nature* **613**, 274–279 (2023).
40. Jiang, J. F. et al. Yttrium-doping-induced metallization of molybdenum disulfide for ohmic contacts in two-dimensional transistors. *Nat. Electron.* **7**, 545–556 (2024).
41. Zou, T. et al. High-performance solution-processed 2D p-Type WSe₂ transistors and circuits through molecular doping. *Adv. Mater.* **35**, 2208934 (2023).
42. Wang, Y. X. et al. Field-effect transistors made from solution-grown two-dimensional tellurene. *Nat. Electron.* **1**, 228–236 (2018).
43. Zhao, C. et al. Evaporated tellurium thin films for p-type field-effect transistors and circuits. *Nat. Nanotechnol.* **15**, 53–58 (2020).
44. Liu, A. et al. Selenium-alloyed tellurium oxide for amorphous p-channel transistors. *Nature* **629**, 798–802 (2024).
45. Subramanian, S. et al. First monolithic integration of 3D complementary FET (CFET) on 300 mm wafers. in *Proc. IEEE Symposium on VLSI Technology*, 1–2 (IEEE, 2020).
46. Schuddinck, P. et al. PPAC of sheet-based CFET configurations for 4 track design with 16 nm metal pitch. in *Proc. IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, 365–366 (IEEE, 2022).
47. Vandoreen, A. et al. Demonstration of 3D sequential FD-SOI on CMOS FinFET stacking featuring low temperature Si layer transfer and top tier device fabrication with tier interconnections. in *Proc. IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, 330–331 (IEEE, 2022).
48. Franco, J. et al. Atomic hydrogen exposure to enable high-quality low-temperature SiO₂ with excellent pMOS NBTI reliability compatible with 3D sequential tier stacking. in *Proc. IEEE International Electron Devices Meeting (IEDM)*, 31.32.31–31.32.34 (IEEE, 2020).
49. Kim, S. K. et al. Heterogeneous 3D sequential CFET with Ge (110) nanosheet p-FET on Si (100) bulk n-FET by direct wafer bonding. in *Proc. International Electron Devices Meeting (IEDM)*, 20.1.1–20.1.4 (IEEE, 2022).
50. Lu, C. M. V. et al. Key process steps for high performance and reliable 3D sequential integration. in *Proc. Symposium on VLSI Technology*, T226–T227 (IEEE, 2017).
51. Huang, C. Y. et al. 3-D self-aligned stacked NMOS-on-PMOS nanoribbon transistors for continued Moore's law scaling. in *Proc. IEEE International Electron Devices Meeting (IEDM)*, 20.6.1–20.6.4 (IEEE, 2020).
52. Kim, S. K. et al. Role of inter-Layer dielectric on the electrical and heat dissipation characteristics in the heterogeneous 3D sequential CFETs with Ge p-FETs on Si n-FETs. in *Proc. International Electron Devices Meeting (IEDM)*, 1–4 (IEEE, 2023).
53. Vandoreen, A. et al. 3D sequential low temperature top tier devices using dopant activation with excimer laser anneal and strained silicon as performance boosters. in *Proc. IEEE Symposium on VLSI Technology*, 1–2 (IEEE, 2020).
54. Chang, S. W. et al. First demonstration of heterogeneous IGZO/Si CFET monolithic 3-D integration with dual work function gate for ultralow-power SRAM and RF applications. *IEEE Trans. Electron Devices* **69**, 2101–2107 (2022).
55. Hsieh, W. H. et al. Monolithic 3-D self-aligned heterogeneous nanosheet channel complementary FETs with matched VT by band alignments of individual channels. in *Proc. IEEE Transactions on Electron Devices*, 3383–3389 (IEEE, 2024).

56. Mertens, H. et al. Nanosheet-based complementary field-effect transistors (CFETs) at 48 nm gate pitch, and middle dielectric isolation to enable CFET inner spacer formation and multi-vt patterning. in *Proc. IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, 1–2 (IEEE, 2023).
57. Jang, D., Jung, S. G., Min, S. J. & Yu, H. Y. Electrothermal characterization and optimization of monolithic 3D complementary FET (CFET). *IEEE Access* **9**, 158116–158121 (2021).
58. Liao, S. et al. Complementary field-effect transistor (CFET) demonstration at 48 nm gate pitch for future logic technology scaling. in *Proc. International Electron Devices Meeting (IEDM)*, 1–4 (IEEE, s2023).
59. Demuyne, S. et al. Monolithic complementary field effect transistors (CFET) demonstrated using middle dielectric isolation and stacked contacts. in *Proc. IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, 1–2 (2024).
60. Ryckaert, J. et al. The complementary FET (CFET) for CMOS scaling beyond N3. in *Proc. IEEE Symposium on VLSI Technology*, 141–142 (IEEE, 2018).
61. Rosseel, E. et al. Source/drain epitaxy for nanosheet-based CFET devices. *ECS Trans.* **114**, 29 (2024).
62. Lee, D., Choi, Y., Kim, J. & Kim, J. Recessed-channel WSe₂ field-effect transistor via self-terminated doping and layer-by-layer etching. *ACS Nano* **16**, 8484–8492 (2022).
63. Das, S. et al. Transistors based on two-dimensional materials for future integrated circuits. *Nat. Electron.* **4**, 786–799 (2021).
64. Cao, W. et al. The future transistors. *Nature* **620**, 501–515 (2023).
65. Wang, S. et al. Two-dimensional devices and integration towards the silicon lines. *Nat. Mater.* **21**, 1225–1239 (2022).
66. Guimaraes, M. H. D. et al. Atomically thin ohmic edge contacts between two-dimensional materials. *ACS Nano* **10**, 6392–6399 (2016).
67. Song, S. et al. Atomic transistors based on seamless lateral metal-semiconductor junctions with a sub-1-nm transfer length. *Nat. Commun.* **13**, 4916 (2022).
68. Jourdain, A. et al. Extreme wafer thinning and nano-TSV processing for 3D heterogeneous integration. in *Proc. IEEE 70th Electronic Components and Technology Conference (ECTC)*, 42–48 (IEEE, 2020).
69. Salahuddin, S., Ni, K. & Datta, S. The era of hyper-scaling in electronics. *Nat. Electron.* **1**, 442–450 (2018).
70. Zhang, D. & Lu, J. J. Q. *Materials for Advanced Packaging 3D Integration Technologies: An Overview*, 1–26 (Springer, 2017).
71. Duan, F. Q. et al. Efficient modulation of thermal transport in two-dimensional materials for thermal management in device applications. *Nanoscale* **15**, 1459–1483 (2023).
72. Zhao, W. et al. Defect-engineered heat transport in graphene: a route to high efficient thermal rectification. *Sci. Rep.* **5**, 11962 (2015).
73. Chen, X. K., Zeng, Y. J. & Chen, K. Q. Thermal transport in two-dimensional heterostructures. *Front. Mater.* **7**, 578791 (2020).
74. Yan, Z. Q., Yoon, M. & Kumar, S. Influence of defects and doping on phonon transport properties of monolayer MoSe₂. *2D Mater.* **5**, 031008 (2018).
75. Zhang, G. & Zhang, Y. W. Strain effects on thermoelectric properties of two-dimensional materials. *Mech. Mater.* **91**, 382–398 (2015).
76. Chu, C. L. et al. Stacked SiGe nanosheets p-FET for Sub-3 nm logic applications. *Sci. Rep.* **13**, 9433 (2023).
77. Arimura, H. et al. Toward high-performance and reliable Ge channel devices for 2 nm node and beyond. in *Proc. IEEE International Electron Devices Meeting (IEDM)*, 2.1.1–2.1.4 (IEEE, 2020).
78. Liu, Y. et al. Promises and prospects of two-dimensional transistors. *Nature* **591**, 43–53 (2021).
79. Hu, C.-K. & Harper, J. M. E. Copper interconnections and reliability. *Mater. Chem. Phys.* **52**, 5–16 (1998).
80. Kotsugi, Y. et al. Atomic layer deposition of Ru for replacing Cu-interconnects. *Chem. Mater.* **33**, 5639–5651 (2021).
81. Han, H. J. et al. Topological metal MoP nanowire for interconnect. *Adv. Mater.* **35**, 2208965 (2023).
82. Chudzik, M. et al. High-performance high-κ/Metal gates for 45nm CMOS and beyond with gate-first processing. *Digest of Technical Papers. 2007 IEEE Symposium on VLSI Technology*, 194–195 (IEEE, 2007).
83. Hinkle, C. L. et al. Dipole controlled metal gate with hybrid low resistivity cladding for gate-last CMOS with low V_t. in *Proc. Symposium on VLSI Technology*, 183–184 (IEEE, 2010).
84. Cheema, S. S. et al. Giant energy storage and power density negative capacitance superlattices. *Nature* **629**, 803–809 (2024).
85. Hu, C. 3D FinFET and other sub-22 nm transistors. in *Proc. 19th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits*, 1–5 (IEEE, 2012).
86. Jeong, J. et al. World's first GAA 3 nm foundry platform technology (SF3) with novel multi-bridge-channel-FET(MBCFET™) process. in *Proc. IEEE Symposium on VLSI Technology and Circuits*, 1–2 (IEEE, 2023).
87. Kim, J. V. et al. S-RCAT (sphere-shaped-recess-channel-array transistor) technology for 70 nm DRAM feature size and beyond. *Digest of Technical Papers. 2005 Symposium on VLSI Technology* 34–35 (IEEE, 2005).
88. Jeon, S., Choi, J., Jung, H.-c., Kim, S. and Lee, T. Investigation on the local variation in BCAT process for DRAM technology. in *Proc. IEEE International Reliability Physics Symposium (IRPS)*, Monterey, CA, USA, FA-4.1–FA-4.2 (IEEE, 2017).
89. Hur, J. S. et al. Oxide and 2D TMD semiconductors for 3D DRAM cell transistors. *Nanoscale Horiz.* **9**, 934–945 (2024).
90. Lee, J. D., Hur, S. H. & Choi, J. D. Effects of floating-gate interference on NAND flash memory cell operation. *IEEE Electron Device Lett.* **23**, 264–266 (2002).
91. Park, K. T. et al. Three-dimensional 128 Gb MLC vertical NAND flash memory with 24-WL stacked layers and 50 MB/s high-speed programming. *IEEE J. Solid-State Circuits* **50**, 204–213 (2015).
92. Huo, Z., Cheng, W. & Yang, S. Unleash scaling potential of 3D NAND with innovative Xtacking® architecture. in *Proc. IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, 254–255 (IEEE, 2022).
93. Auth, C. et al. A 10 nm high performance and low-power CMOS technology featuring 3rd generation FinFET transistors, Self-Aligned Quad Patterning, contact over active gate and cobalt local interconnects. in *Proc. IEEE International Electron Devices Meeting (IEDM)*, 29.1.1–29.1.4 (IEEE, 2017).
94. Beyne, E., Jourdain, A. and Beyer, G. Nano-through silicon vias (nTSV) for backside power delivery networks (BSPDN). in *Proc. IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, 1–2 (IEEE, 2023).
95. Abedin, M., Khan, S., Lanzillo, N. & Dechene, D. DTCO guided process integration: case studies from FEOL & BEOL with BSPDN. in *Proc. 35th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)*, 1–5 (IEEE, 2024).
96. Zhang, X. W. et al. Heterogeneous 2.5D integration on through silicon interposer. *Appl. Phys. Rev.* **2**, 021308 (2015).
97. Zhang, S. et al. Challenges and recent perspectives of 3D heterogeneous integration. *e-Prime Adv. Electr. Eng. Electron. Energy* **2**, 100052 (2022).
98. Munoz, R. Industry scale reuse in the chiplet Era. in *Proc. International VLSI Symposium on Technology, Systems and Applications, 2023 International VLSI Symposium on Technology, Systems and Applications (VLSI-TSA/VLSI-DAT)*, 1–2 (IEEE, 2023).

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H.H.Y., J.Y.P., Y.T.M., and J.H.B. contributed equally to this work. H.H.Y., J.Y.P., Y.T.M., J.H.B., M.S., D.-H.K., and H.-J.S. researched data for the article, and H.H.Y., D.-H.K., and H.-J.S. wrote the manuscript. D.A. and D.H. contributed substantially to discussion of the content, and reviewed and/or edited the manuscript. D.A., D.H., D.-H.K., and H.-J.S. supervised the work.

Competing interests

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