Received: 19 February 2025 | Revised: 13 March 2025 | Accepted: 17 March 2025

DOI: 10.1002/jsid.2068

WILEY

INVITED PAPER

Effective 10-bit OLED driver IC with 11-bit DAC, double capacitor-coupled adder, and offset calibration for enhanced panel driving

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Abstract

In this paper, we propose an 11-bit source driver IC optimized for high-resolution OLED display driving. The proposed IC adopts a Double Capacitor Coupled Adder (DCCA) structure, which enables parallel execution of the sampling and driving stages, thereby improving temporal efficiency and response speed. Additionally, we introduce a novel Slew Rate Enhancement (SRE) structure that enables rapid response even in conditions with minimal input–output voltage differences, delivering performance well-suited for high-resolution display driving. An Offset Calibration circuit is included to minimize inter-channel voltage discrepancies, ensuring high precision and consistent output performance. Experimental results demonstrate that the proposed IC achieves a short horizontal line time(H) of 2.0 μs and a slew rate of 9.9 V/μs. The differential nonlinearity (DNL) and integral nonlinearity (INL) are 0.66 LSB and 0.98 LSB, respectively, and, after Offset Calibration, the maximum inter-channel deviation of output voltage (DVO) is reduced to 2.43 mV.

KEYWORDS

deviation of voltage outputs, double capacitor-coupled adder, offset calibration, OLED driver IC, slew rate enhancement, source driver

1 | INTRODUCTION

With the recent advancements in Organic Light-emitting Diode (OLED) display driving technology, there is an increasing demand for high-performance driver ICs capable of accurately and stably driving panels at high resolutions and frame rates. In response to this demand, Umeda et al. were the first to propose a Liquid Crystal Display (LCD) driver with a capacitor-coupled adder, introducing an effective method for performing sampling and driving in analog signal processing.[1] Additionally, Huang et al. improved area efficiency by proposing a 12-bit structure that sums three voltages.[2] However, these designs require sequential sampling and driving within a 1-H interval, resulting in time constraints. Meanwhile, Jo et al. proposed a High-Gain Fast-Slew Circuit for high-resolution and high-frame-rate OLED displays, but this approach has a limitation in that the slew detector only activates when the input–output voltage difference exceeds the threshold voltage.[3] In addition to these efforts, various other techniques have also been explored to enhance the slew rate of source drivers, aiming to

improve overall display performance and power efficiency.[4–8]

In recent studies, minimizing the DVO has emerged as a key criterion for evaluating driver IC performance. A low DVO indicates high inter-channel voltage uniformity, which is crucial for enhancing display image quality.[9] Previously, techniques such as chopping have been employed in source drivers to reduce DVO, effectively making the amplifier's offset imperceptible to the human eye.[10] However, with the growing focus on power efficiency, recent research has actively explored methods to adjust the refresh rate dynamically.[11–13] In such cases, the refresh rate can be reduced to as low as 1 Hz, making it impossible to apply conventional chopping-based techniques. To overcome this limitation, this paper introduces a novel offset calibration technique.

To overcome the limitations of prior designs, this paper proposes a structure that uses two capacitors to allow the sampling and driving phases to occur simultaneously, thereby improving temporal efficiency. Additionally, we present a SRE circuit capable of responding quickly even when input–output voltage differences are minimal, achieving the fast response speed and stability required for high-resolution display driving. To further improve performance, our design employs Offset Calibration, achieving a low DVO value and enhancing output uniformity across channels.

In this paper, Section 2 describes the proposed OLED driver IC architecture and design methodology. Section 3 introduces the novel DCCA and explains its operating principles. Section 4 presents the offset calibration circuit, detailing how it enhances voltage uniformity. Section 5 discusses the SRE circuit and its impact on response speed. Section 6 provides experimental results and performance comparisons with prior works. Finally, Section 7 concludes the paper and suggests directions for future research.

2 | PROPOSED DRIVER IC

Figure 1 shows the block diagram of the proposed OLED driver IC designed to achieve both high-precision voltage control and high-speed operation for high-resolution OLED displays. The IC adopts an 11-bit resolution architecture, where 10 bits are used to generate pixel voltages, and an additional 1 bit is allocated for offset correction to compensate for channel-to-channel variations and improve channel uniformity.

The input data from the T-Con is sequentially transferred to each channel through the shift register, and these input data are transferred from the low voltage domain to the middle voltage domain through the level shifter. Then,

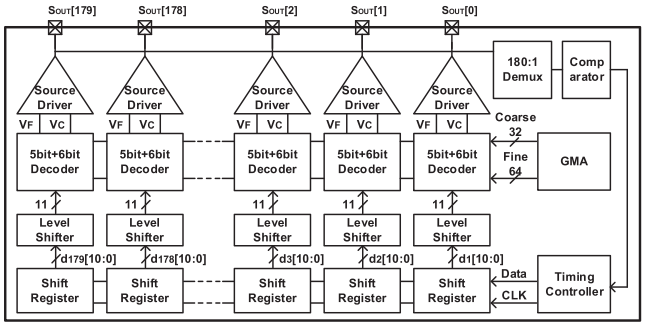

FIGURE 1 Block diagram of the proposed OLED driver IC.

a 5-bit + 6-bit decoder converts the digital input into two voltage components, the coarse voltage (V_C) and the fine voltage (V_F). The coarse voltage (V_C) is generated by selecting one of 32 voltage levels from the resistor ladder, while the fine voltage (V_F) is obtained through a secondary 64-level sub-DAC to ensure fine granularity in the output voltage control. These voltages are then transferred to the DCCA to generate the final pixel driving voltages and deliver them to the display panel.

To ensure uniform output across all channels, the proposed IC integrates an offset correction process. A comparator-based feedback loop detects the voltage difference between channels and transmits the correction value to the timing controller (T-Con). The T-Con then adjusts the voltage of each channel appropriately to minimize the deviation. The offset correction circuit operates by sequentially connecting each of the 180 source driver channels to a single comparator using a 180:1 demultiplexer (Demux), thereby enabling efficient error correction without the need for a dedicated comparator for each channel. This method effectively reduces the DVO from 12.99 mV to 2.43 mV, ensuring consistent grayscale accuracy and image quality across the display.

In addition to high-precision voltage control, the proposed IC is optimized for high-speed operation. This architecture ensures that the sampling and driving stages occur simultaneously, improving time efficiency compared to conventional designs that require these operations to be executed sequentially. High-speed shift registers allow smooth data propagation, while level shifters ensure that the decoded signal is appropriately amplified to match the required driving voltage range. The timing controller plays a critical role in synchronizing data transmission, decoding, and output control, ensuring stable operation even at high refresh rates.

By integrating these functions, the proposed OLED driver IC achieves fast response time, low power consumption, and improved display uniformity, making it a very suitable solution for next-generation high-resolution OLED panels.

3 | CAPACITOR COUPLED ADDER

Figure 2 shows the block diagram of the proposed 11-bit R-Ladder DAC. Unlike the conventional structure that requires sequential sampling and conversion processes, it provides both area efficiency and high-speed response performance by performing them in parallel with two capacitors for sampling and driving. In addition, it eliminates the influence caused by charging V_C and V_F simultaneously in the sampling stage by using two resistor strings and makes sampling faster.

Figure 3 shows the operation of the proposed DCCA, depicting the circuit configuration for each operation mode and its corresponding timing diagram. In the Reset Mode, capacitors C1 and C2 are initialized using the Φ_{rst} signal, ensuring that previous charge residues do not interfere with subsequent operations.

During the 1H phase, V_C and VF are sampled at the positive and negative terminals of C1, respectively. To minimize the impact of clock feedthrough on V_F, which requires higher precision, the Φ_{1e} switch opens earlier than the Φ_1 switch. As a result, C1 stores the voltage difference between V_C and V_F.

During the 2H phase, the stored charge is transferred to the amplifier input while simultaneously sampling the next input using C2. This interleaving operation allows the system to fully utilize the entire horizontal period for both sampling and driving, thereby improving temporal efficiency. At this stage, the output voltage can be expressed as follows:

$$V_{OUT} = V_C - V_F + V_{MID} \quad (1)$$

The proposed DCCA structure leverages two capacitors, allowing the full 1-H period to be utilized for both sampling and driving. This design achieves both temporal efficiency and high-speed response.

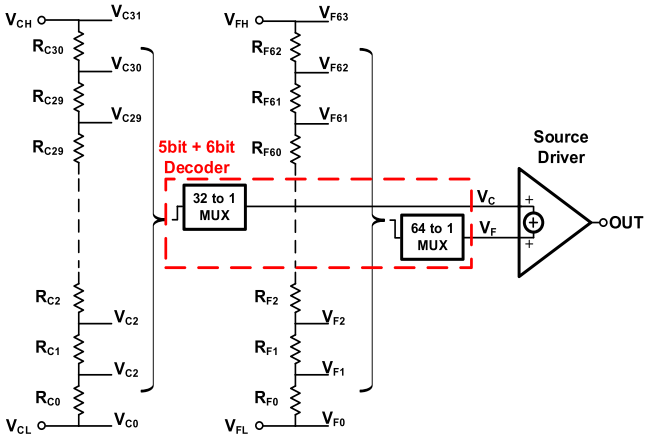

FIGURE 2 Block diagram of the 11bit R-ladder DAC.

4 | AMP OFFSET CALIBRATION

Figure 4 shows the operating principle of the proposed offset calibration circuit. The purpose of this circuit is to determine the appropriate dn[5:0] value that allows the VF output from the Fine R-string to be set as $V_{MID} + V_{offset}$, where V_{offset} represents the amplifier's offset. To achieve this, the upper voltage (V_{FH}) of the fine R-string is set to $V_{MID} + 31\times$LSB, and the lower voltage (V_{FL}) is set to VMID-32×LSB, ensuring that the midpoint value 6'd32 corresponds to V_{MID}.

1. Initial State (Closed-loop Mode)
   - In RST Mode, the amplifier operates as a unity-gain buffer, maintaining a closed-loop state while outputting V_{MID}.

1. Transition to Open-loop Mode and Offset Detection
   - The V_F voltage is connected to the negative input terminal, transitioning the amplifier into an open-loop state.

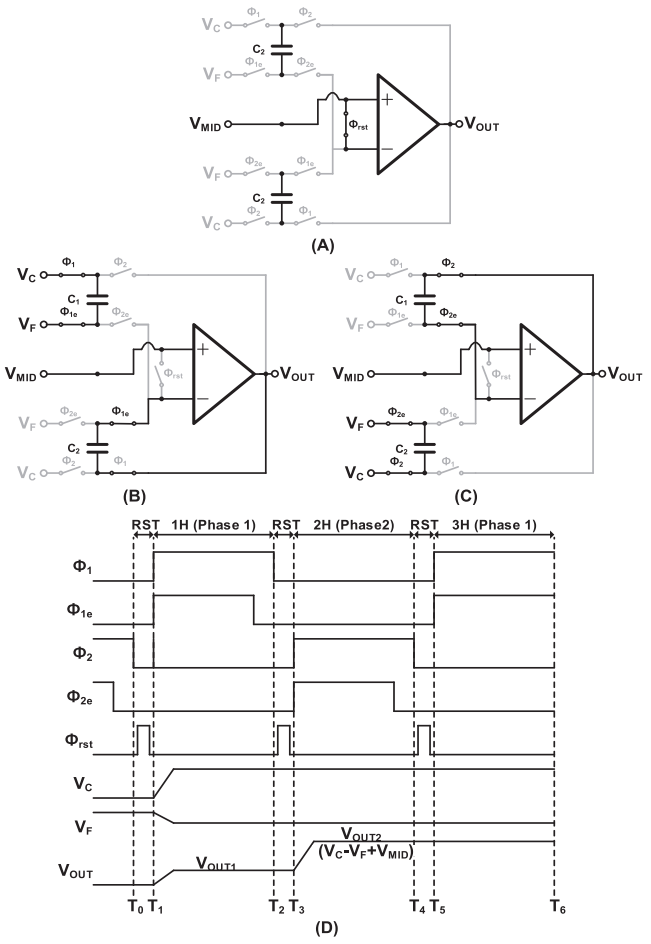

FIGURE 3 Operation of proposed double capacitor coupled adder (a) reset mode (b) 1 H (c) 2 H (d) timing diagram.

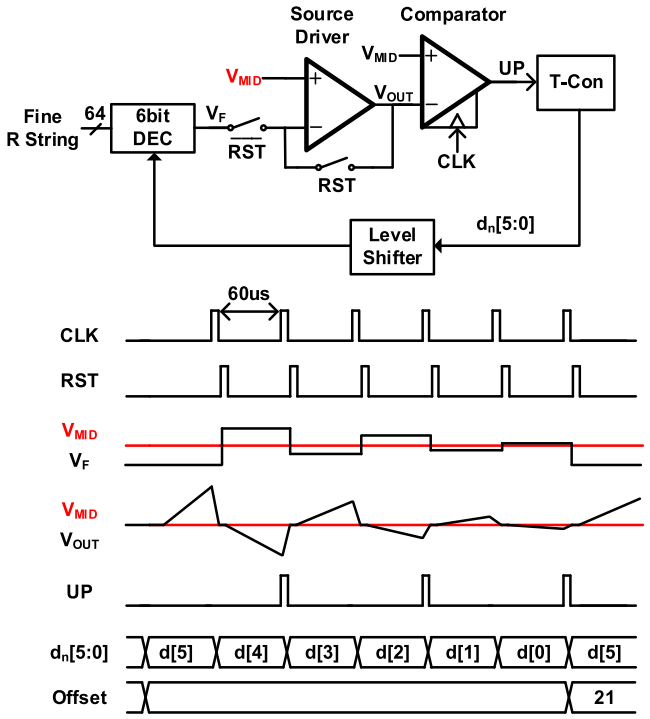

FIGURE 4 Principle of amp offset calibration.

- In the open-loop state, the amplifier's output is amplified proportionally to the input voltage difference, resulting in a relatively large offset value.
- Considering PVT (Process, Voltage, Temperature) variations, the amplifier is designed to achieve a minimum gain of 60 dB at 20 kHz. After approximately 60 μs of amplification, the signal is amplified by a factor of at least 1,000 times.

2. Offset Calibration using a comparator
   - A 180:1 Demux connects 180 source channels to a single comparator, ensuring that all channels share a consistent comparator offset.
   - The comparator compares the difference between V_{OUT} of the amplifier and V_{MID}.
   - Based on the comparison results, an UP signal is generated, updating the dn[5:0] code to correct the offset.

3. The final corrected offset value is stored in a register and is periodically applied to each channel by the T-Con.

5 | SLEW RATE ENHANCEMENT

Conventional SRE circuits have the advantage that no static current flows once the amplifier's settling is complete.[3] However, they have a limitation in that V_{IN} – V_{OUT} must be greater than the threshold voltage for the slew detector to active. To overcome this limitation, this paper proposes an operational transconductance amplifier (OTA)-based architecture that amplifiers current even for small input–output voltage differences, enabling faster response.

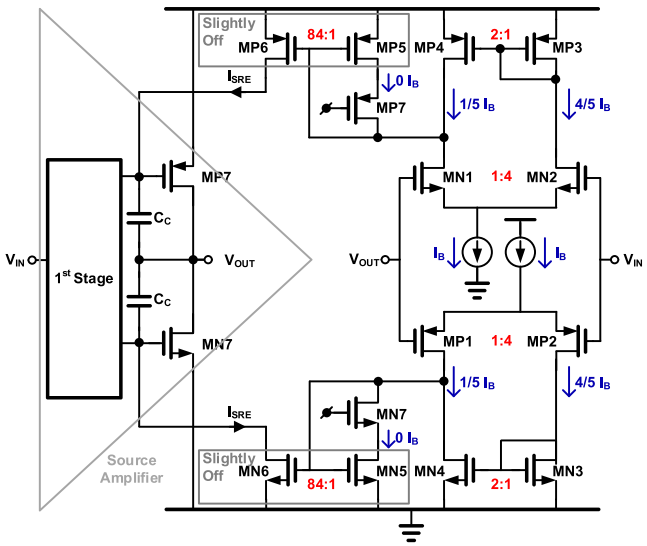

FIGURE 5 Schematic of source driver with slew rate.

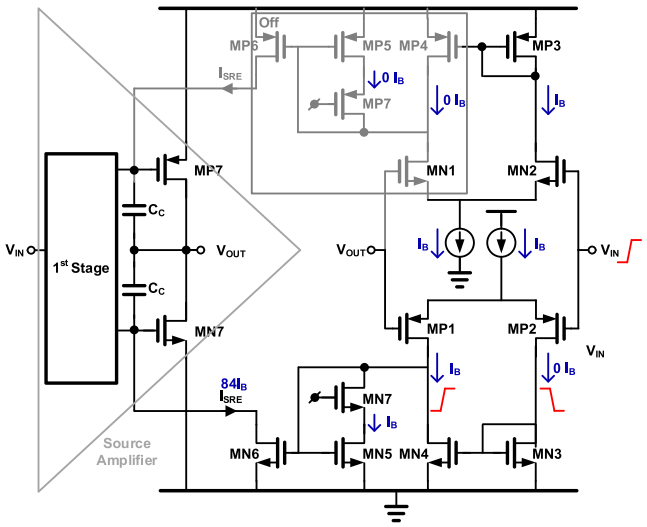

FIGURE 6 Principle of source driver with slew rate enhancement.

Figure 5 shows the schematic of the proposed SRE function integrated into the source driver. Unlike OTAs, the sizes of the input transistors and their current ratios are deliberately mismatched. This design allows the SRE to turn off quickly, preventing excessive oscillation during the settling. Additionally, when settling is complete and V_{OUT} equals V_{IN}, the drain voltages of MN4 and

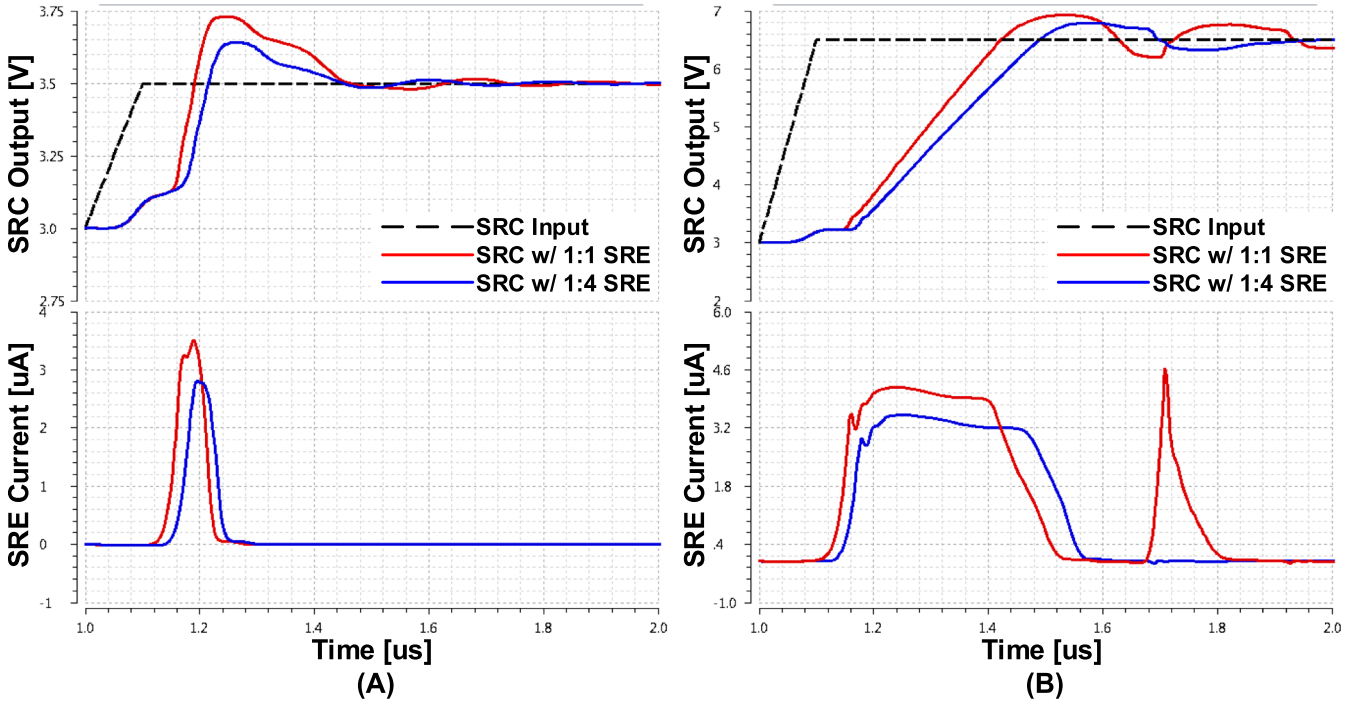

FIGURE 7 Simulated output voltage of the source driver based on the size ratio of the SRE and the output swing of the source driver.

MP4 are designed to be very close to VSS and VDD, respectively, preventing unwanted current flow through MN6 and MP6. If static current flows through MN6 and MP6, the operating point of the core amplifier is disrupted, which can critically affect system stability.

Figure 6, shows the operation of SRE when the input voltage rises. The width and length of MN6 and MP6 are set to 21 times and 1/4, respectively, compared to MN5 and MP5. This configuration maximizes I_{SRE}, allowing up to $84I_B$ to flow.

Figure 7 presents simulation results demonstrating the impact of the input transistor size ratio on SRE performance. Since MP4 and MN4 must remain off, their size ratio is maintained at 2:1. While SRE operates even with a 1:1 input transistor size ratio, as shown in Figure 7A, this configuration results in excessive overshooting. Furthermore, as seen in Figure 7B, after the rising transition, the SRE current does not fully turn off, leading to a settling delay. To mitigate these issues and achieve optimal SRE performance, this paper proposed an input transistor size ratio of 4:1.

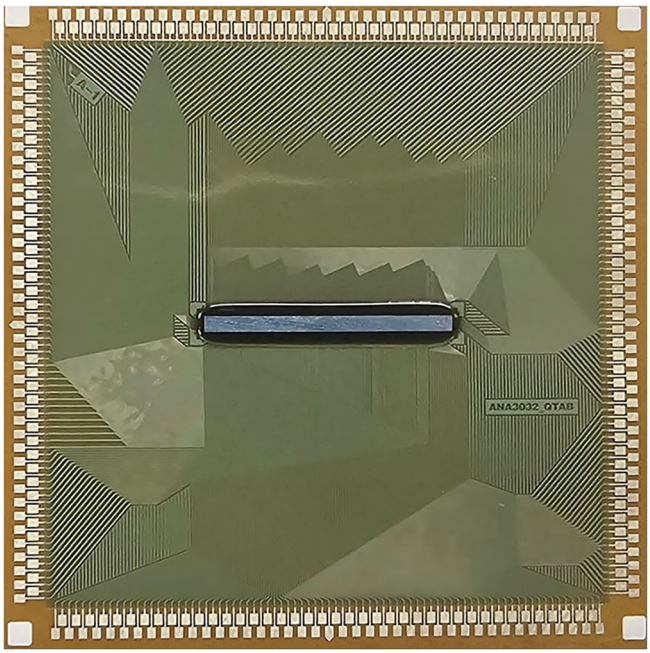

FIGURE 8 Die photograph with COF package.

6 | MEASUREMENT RESULTS

Figures 10–13 show the measurement results of six channels of the proposed OLED driver IC, presenting linearity, offset calibration, and output waveforms. Figures 8 and 9 show the die photograph and micrograph of the

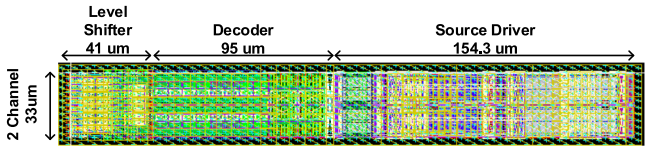

FIGURE 9 Die micrograph of the proposed OLED driver IC.

proposed OLED driver IC. The IC is fabricated using a Chip-on-Film (COF) package, ensuring high integration and optimization for high-resolution displays. The micrograph shows the dimensions of each block, with the level shifter measuring 41 um, the decoder 95 um, and the source driver 154.3 um.

Figure 10 shows the measured linearity performance of the source driver. Figure 10A shows the output characteristics corresponding to the 10-bit input data, confirming that linearity is maintained across the entire input range. Figure 10B shows the INL and DNL performance, both remaining within ±1 LSB and demonstrating monotonic behavior.

Figure 11 shows a comparison of measurement results before SS and after offset calibration. Before calibration, the maximum deviation between channels was 12.99 mV, which was reduced to 2.43 mV after

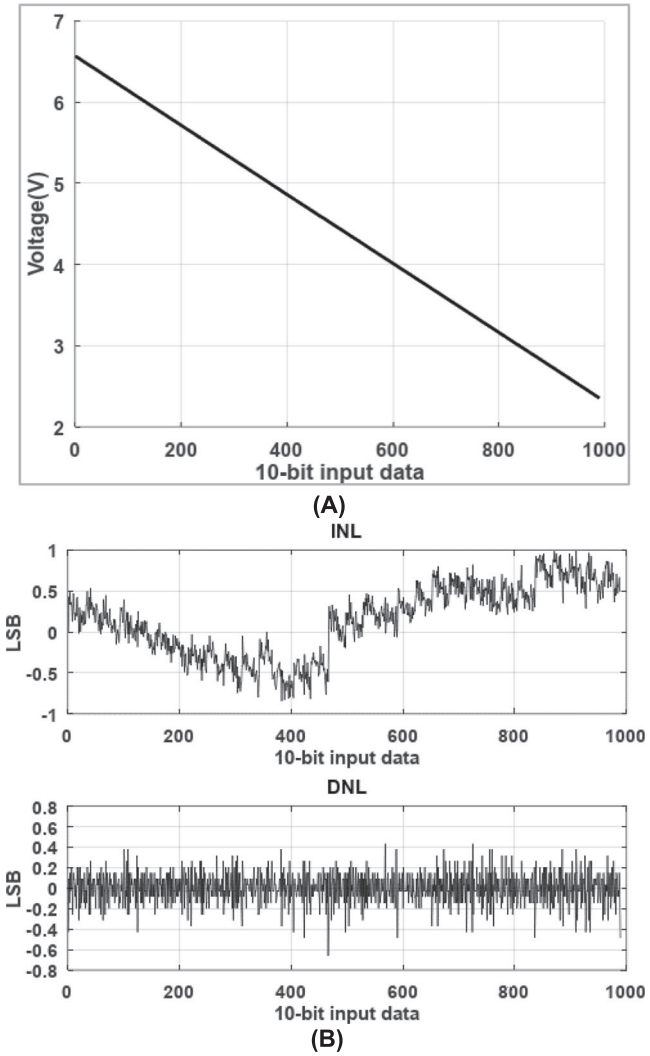

FIGURE 10 Measurement results with for channel proposed driver IC (A) output characteristic (B) INL & DNL.

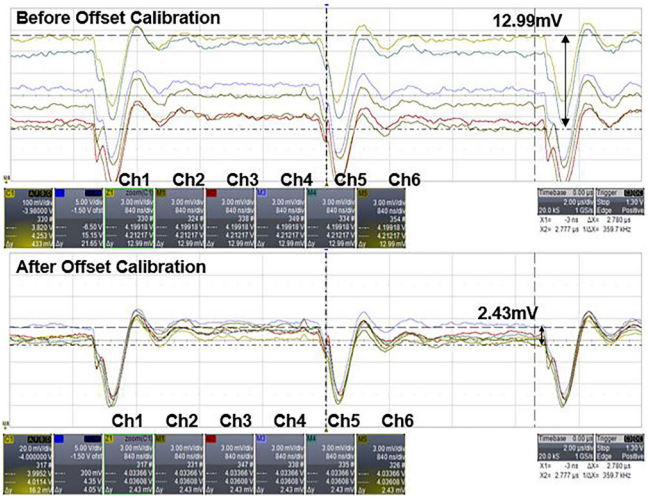

FIGURE 11 Measurement results before and after offset calibration.

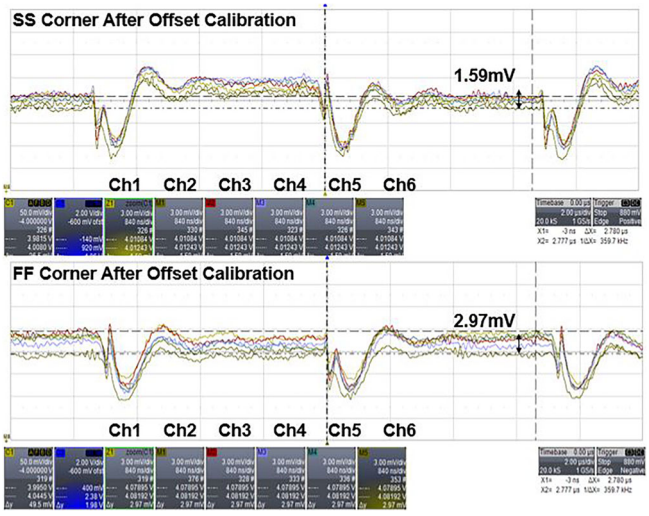

FIGURE 12 Measurement results according to corner variation.

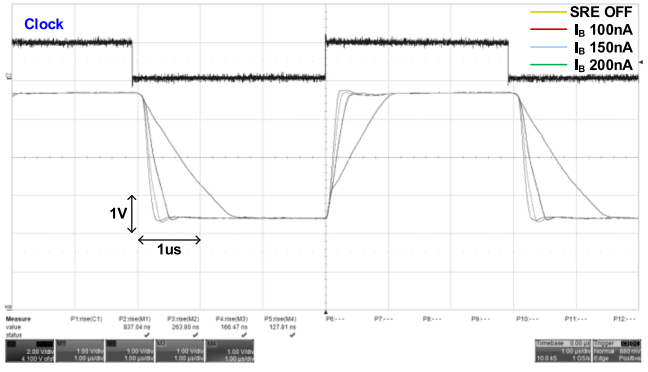

FIGURE 13 Output swing of source driver.

TABLE 1 The performance summary of the proposed OLED driver IC with a comparison table.

	This work	JSID 2024[3]	JSSC 2021[7]	VLSI 2021[8]	JSSC 2023[9]	ISSCC 2024[14]	JSSC 2024[15]
Process	28 nm	28 nm	90 nm	180 nm	130 nm	65 nm	180 nm
Gray Scale	11 bit (5b + 6b)	11b (7b + 4b)	10 bit (10b + 0)	12 bit (7b + 5b)	10 bit (10b + 0)	10 bit (10b + 0)	10bit (6b + 4b)
DAC Architecture	Double Capacitor Adder		Fully R-DAC + SC-amplifier	Piecewise Linear	SC-multiplier +LSB stack-up	Global Slope-DAC	QM-DAC
Line time	2.0 us	2.7 us	3.8 us	2.0 us	8.0 us	8.2 us	1.5 us
Slew Rate	9.9 V/us @46.6 pF	7.645 V/us @54 pF	3.8 V/us @30 pF	6.24 V/us @80 pF	8.1 V/us @30 pF	4.7 V/us @30 pF	22 V/us @100 pF
Static Current (uA/ch)	1.28 uA	1.2uA	2.8 uA	2.0 uA	1.8 uA	1.5 uA	2.4 uA
Output Range (V)	2.56–6.36	3.0–6.8	0.2–4.8	0.1–4.9	0.3–4.5	0.3–4.7	0.25–4.85
DNL/INL (LSB)	0.66/0.98	0.48/0.50	0.2/0.42	0.43/0.95	0.39/0.9	0.49/0.85	0.21/1.21
Max. DVO	13 mV/ *2.43 mV	11 mV	7.9 mV	7.9 mV	4.82 mV	10.0 mV	11.5 mV
Area	4,790 um^2 (290.3 × 16.5)	N/A	4,734 um^2 (263 × 18)	5,015 um^2 (295 × 17)	2,304 um^2 (144 × 16)	2,171 um^2 (135.7 × 16)	3,315 um^2 (221 × 15)

*DVO after offset calibration.

calibration, significantly improving voltage uniformity between channels.

Figure 12 shows the offset calibration results under SS (Slow-Slow) and FF (Fast-Fast) corner process variations. After calibration, the maximum deviation was measured as 1.59 mV in the SS corner and 2.97 mV in the FF corner. These results confirm that the offset calibration was effectively performed across all process conditions.

Figure 13 shows the transient response and slew rate of the source driver. The output voltage swing reaches 3.27 V, and for a 10% to 90% transition, when I_B ranges from 100 nA to 200 nA, the rise time was measured between 264 ns and 128 ns. During this period, the slew rate ranged from 9.9 V/μs to 20.4 V/us. While increasing I_B to 200 nA significantly enhances the slew rate, it may cause excessive overshooting, prolonged settling time, and increased power consumption. Therefore, in this study, I_B was optimized at 100 nA to achieve balanced performance.

7 | CONCLUSION

The proposed OLED Driver IC is designed with an 11-bit resolution architecture based on a 28 nm process, achieving both high resolution and excellent area efficiency compared to conventional structures through the use of a DCCA. This IC provides high precision with an effective output performance corresponding to 10 bits, enabled by offset calibration.

As shown in Table 1, the proposed IC achieves a short line time of 2.0 μs and a stable slew rate of 9.9 V/μs with a load capacitance of 46.6 pF. This represents the fastest slew rate relative to current consumption compared to previous studies. Additionally, after offset calibration, the maximum DVO is reduced to 2.43 mV, demonstrating superior uniformity compared to other studies.

In conclusion, the proposed OLED Driver IC meets high resolution, fast response time, low power consumption, and compact area requirements, making it a promising solution for next-generation high-performance OLED display driving applications.

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How to cite this article: Kim C, Lee S, Lee M. Effective 10-bit OLED driver IC with 11-bit DAC, double capacitor-coupled adder, and offset calibration for enhanced panel driving. J Soc Inf Display. 2025. https://doi.org/10.1002/jsid.2068