

A 13-bit 3-MS/s Asynchronous SAR ADC with a Passive Resistor Based Loop Delay Circuit

Hyungyu Ju and Minjae Lee *

The School of Electrical and Computer Science, Gwangju Institute of Science and Technology, Gwangju 61005, Korea; hgju@gist.ac.kr

* Correspondence: minjae@gist.ac.kr; Tel.: +82-062-715-2205

Received: 9 February 2019; Accepted: 26 February 2019; Published: 27 February 2019

Abstract: An asynchronous successive approximation register (SAR) ADC incorporates a passive resistor based delay cell to reduce power consumption and accommodate the SAR ADC with a reconfigurable sampling frequency or tapered bit period without repeated delay calibration. The ADC aims to have a sampling frequency of several MS/s. The proposed delay cell adopts resistance controlled delay architecture to generate a delay of nanoseconds with high linearity. The resistance controlled delay cell is based on a passive resistor instead of a MOS transistor using a triode region to avoid the nonlinear delay characteristic of active devices. From the analysis of the linearity of delay cell, the passive resistor based delay cell achieves a delay error of about 5 percent. The prototype ADC to validate the proposed passive resistor based delay cell is fabricated in 40 nm CMOS. The ADC occupies 0.054 mm² and achieves an SNDR of 57.4 dB under 67 μ W power dissipation at a 1.1 V supply with a 3 MHz sampling frequency.

Keywords: asynchronous; delay cell; passive resistor; SAR ADC; loop delay circuit

1. Introduction

From low speed applications such as industrial monitoring, bio-medical and sensor node [1–3] to high speed applications such as high speed links and next generation communication systems [4,5], Successive Approximate Register (SAR) ADC is the most widely adopted ADC architecture owing to its low power operation from a simple operating principle. Moreover, an asynchronous architecture is also widely used to mitigate the requirements of the comparison time of the comparator in SAR ADC.

In the asynchronous SAR ADC, the time budget of the sampling clock is composed of an input sample time, comparator comparison time, capacitor DAC settling time, digital logic propagation delay, and the number of repetitions proportional to the resolution, as shown in Figure 1. While many studies have been conducted to reduce each timing budget to enhance the ADC performance, the loop delay that replaces the DAC settling time has been subjected to few methodological studies. Therefore, this paper focuses on digitally controlled delay generation methods with linear delay characteristics when the asynchronous SAR ADC has a sampling frequency of several MS/s. The linear delay characteristics can be applied to design the loop delay circuit of SAR ADC with reconfigurable sampling frequency or tapered bit periods [6,7]. For the SAR ADC of this paper, we designed an ADC with reconfigurable sampling frequency to obtain an adjustable frame rate in a touch screen panel (TSP) readout IC.

There are several ways to implement a digitally controlled variable delay cell. The popular method is a delay cell with shunt capacitors [8]. Assuming that the delay cell is a first-order RC circuit, this delay cell adjusts the capacitance depending on the digital input patterns. Similarly, a method adjusting the resistance in the first-order RC circuit was introduced in reference [9]. An MOS

transistor array was used as a variable resistor. Another method used to generate a digitally controlled delay cell is a current starved architecture [10]. The delay cell adopts a tail current source, thus adjusting delay by digitally controlled current level. Using digital logic propagation delay is another way to implement a digitally controlled delay cell [11]. This method adjusts the delay by varying the number of logic gates.

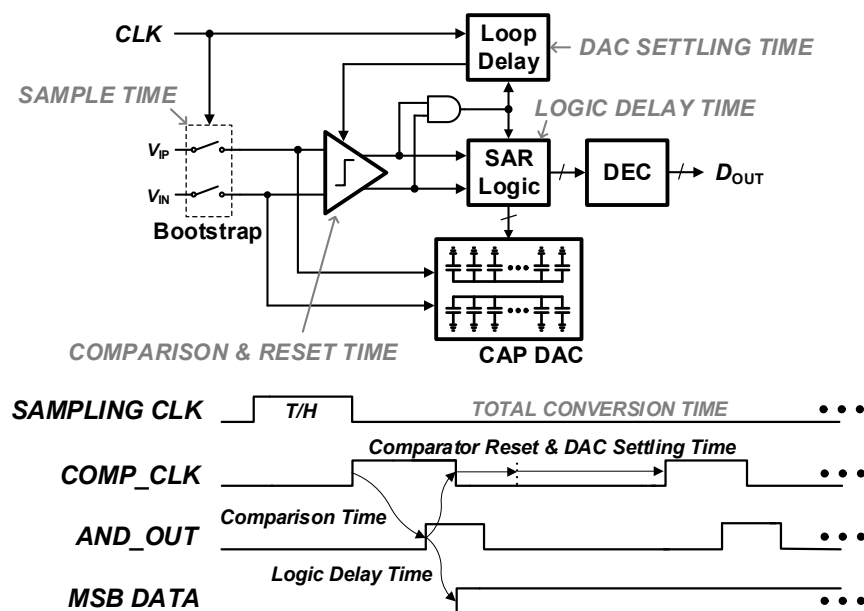


Figure 1. A structure and timing budget of the asynchronous SAR ADC.

When the delay cell is applied to the asynchronous SAR ADC, with sampling frequency of few MS/s and medium resolution, the delay cell should have a delay value of several tens of nanoseconds. Thus, the delay generation methods using the logic propagation delay and variable capacitance are inadequate due to power consumption in proportion to delay. In addition, the current staved structure requires an analog bias voltage, which leads to static current consumption by an additional bias generation circuit. In the case of using a MOS transistor as a variable resistor, the coding problem occurs due to the unpredictable circuit characteristic when the delay is generated by the equivalent resistance value.

Among the methods used to generate delay, the proposed delay cell adopts a resistive controlled delay cell to achieve high linearity with low power consumption. Thus, the proposed delay cell replaces the MOS transistor array to passive resistors to avoid the nonlinear delay characteristic and code dependent parasitic capacitance of the active device. The structure of the proposed delay cell is described in Section 2, along with the analysis of the linearity of the delay. The detailed circuit implementation of the proposed delay cell is represented in Section 3 with a delay calibration method. Finally, the simulation and measurement results are shown in Section 4, and we conclude the paper in Section 5.

2. Linearity of Delay Cell

Figure 2 shows a simple delay cell structure with a RC low-pass filter. When the input changes from high to low, the output voltage $V_{OUT}(t)$ can be expressed as a first order response given as

$$V_{out}(t) = V_{sup}(1 - e^{-t/\tau}) \quad (1)$$

where V_{sup} is supply voltage of delay cell. Then, we can solve the (1) for t , yielding

$$t = \tau \ln \frac{V_{sup}}{V_{sup} - V_{out}(t)} \quad (2)$$

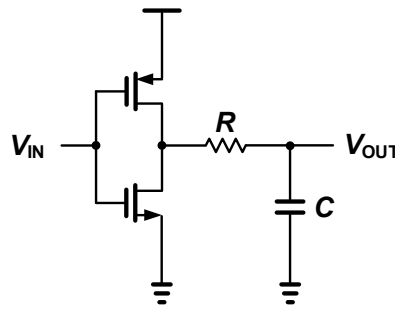


Figure 2. Simple delay cell using a passive resistor and capacitor.

Assuming that a logical signal is delivered to the next digital logic when the voltage settling is about 50 percent, the final value of $V_{out}(t)$ can be approximated to be $0.5 V_{sup}$. Then, the logarithm term in (2) can be replaced by a constant coefficient α . Thus, the calculated delay time for the time constant can be expressed as

$$t = \alpha \cdot \tau = \alpha \cdot (R_{on,p} + R)C \quad (3)$$

where $R_{on,p}$ is the turn on resistance of the P-type MOS transistor. From (3), the resistance R , capacitance C and equivalent resistance of the MOS transistor $R_{on,p}$ are the factors that can adjust the delay time. However, adjusting C is difficult, because the power consumption of delay cell is proportional to C . In addition, using turn on resistance $R_{on,p}$ of the transistor is also not suitable due to the poor linearity of delay from the nonlinear characteristic of active devices. Therefore, adjusting R is the most reasonable approach in terms of power consumption and delay linearity. Then, we obtain a linear delay step according to the derivation of R which is given as

$$\Delta t = \alpha \cdot \Delta \tau = \alpha \cdot \Delta RC \quad (4)$$

It is important that the effect on $R_{on,p}$, which causes the nonlinearity, is eliminated in the resistive controlled delay cell.

The proposed digitally controlled delay cell is shown in Figure 3. The resistance is controlled by a switch with a small resistance value. C_p is the parasitic capacitance of the switch. As the switch is made of a pass transistor, the parasitic capacitance changes depending on whether the switches are on or off. $C_{p,tot}$ is sum of the parasitic capacitances for all pass transistors.

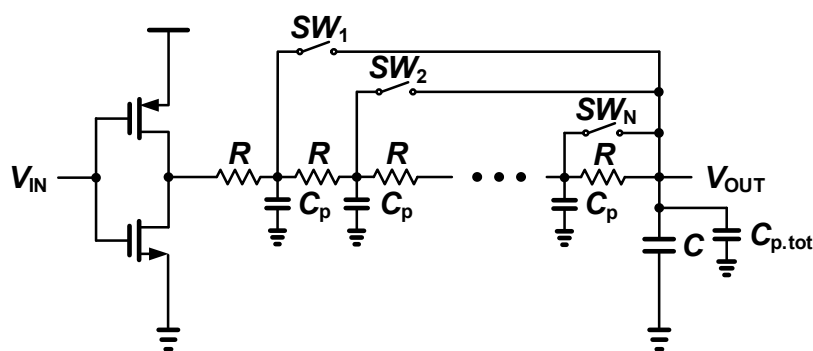


Figure 3. Proposed resistive controlled delay cell.

From (3) the delay time is calculated by the product of time constant of the circuit and constant coefficient α . In other words, we can obtain the delay time by calculating the time constant of delay cell. To derive the time constant of entire RC network of proposed delay circuit, the Elmore delay model is employed.

Figure 4 represents the RC network model of proposed delay cell. $R_{on,ptr}$ is the turn on resistance of a switch made of pass transistor. $C_{p,on}$ and $C_{p,off}$ are parasitic capacitances of turn on and off switch, respectively. Among the switches, only one switch is turned on as the digital control

input, so the internal RC network connected in parallel with the $R_{on.ptr}$ must be converted to a network, to which the Elmore delay model is applicable.

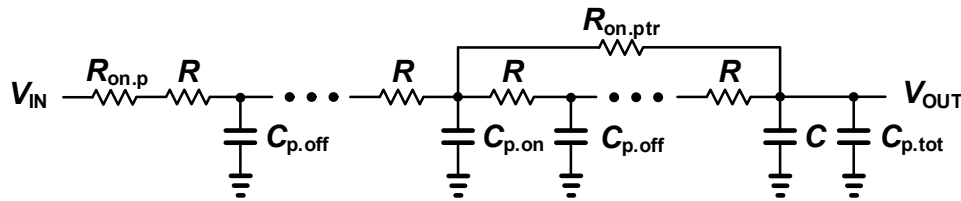


Figure 4. RC network model of proposed delay cell.

To simplify the internal RC network, Figure 5 describes a lumped PI-T transform method [12]. After calculating the time constant of PI and T model using Elmore delay model, two relations of the lumped PI-T transform are given as

$$R_P = 2R_T, C_T = 2C_P \quad (5)$$

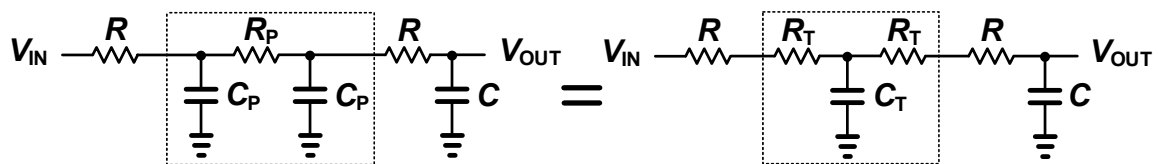


Figure 5. Lumped PI-T transform.

Using the lumped PI-T transform, the internal RC network can be simplified in the form of PI, and the parameters of the simplified PI model R_P and C_P are calculated as

$$R_P = kR, C_P = 0.5(k-1)C_{p.off} \quad (6)$$

where k is the number of R in the internal RC network.

Figure 6 shows the RC network model of proposed delay cell using (6). N represents the total number of switches. Assuming that $R_{on.ptr}$ is much smaller than R , the resistance of parallel resistors can be approximated as

$$(N-k+1)R \parallel R_{on.ptr} \approx R_{on.ptr} \quad (7)$$

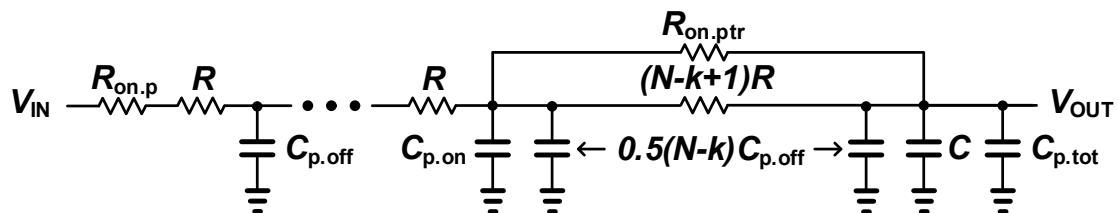


Figure 6. Equivalent RC network model of proposed delay cell.

Then, the normalized time constant equation of the proposed delay cell can be obtained as

$$\tau_k = g(k) + (R_{on.p} + kR)(C_{p.on} + 0.5(N-k)C_{p.off}) + (R_{on.p} + kR + R_{on.ptr})(C + C_{p.tot} + 0.5(N-k)C_{p.off}) \quad (8)$$

where

$$g(k) = \begin{cases} 0, & k = 1 \\ \sum_{i=1}^{k-1} (R_{on.p} + iR)C_{p.off}, & k \geq 2 \end{cases}$$

Finally, the delay step can be obtained by the difference between the previous and current step of the normalized time constant from (4) and is derived as

$$\begin{aligned}\Delta t &= \alpha \cdot (\tau_k - \tau_{k-1}) \\ &= \alpha \cdot [R(C + C_{p.tot} + C_{p.on} + (N + 1)C_{p.off} - 0.5kC_{p.off}) - 0.5R_{on.ptr}C_{p.off}]\end{aligned}\quad (9)$$

It is important to note that the nonlinearity of proposed delay cell is determined by the term multiplied by the value of k . If N is large enough, Equation (9) can be approximated as

$$\Delta t \cong \alpha \cdot [R(C + 2C_{p.tot} - 0.5kC_{p.off})]\quad (10)$$

The term including $R_{on.ptr}$ is very small and hence negligible. If C is not in (10), then the delay linearity of the proposed structure has an error of approximately ± 12.5 percent at maximum. In order to attain more linearity, the passive capacitor C is added at the cost of the increased power consumption.

3. Circuit Implementation

The implementation of loop delay circuit for asynchronous SAR ADC is presented in Figure 7. This circuit senses the comparison completion of the comparator and makes the comparator reset and operation clock repeatedly. The detailed circuit operation is as follows. When the START generated by inverting the sampling clock goes high, the loop is activated and the first comparison is made as the comparator clock COMP_CLK goes high. After the comparison of the comparator, the COMP_DONE indicating the end of the comparison becomes high and quickly resets COMP_CLK through the comparator reset path. As the comparator is reset, COMP_DONE is also reset. Then, the low state of COMP_DONE is propagated through DAC settling path, and COMP_CLK becomes high again after a propagation delay of delay cell. This SAR operation loop is repeated until the STOP goes high after all conversion cycles have ended.

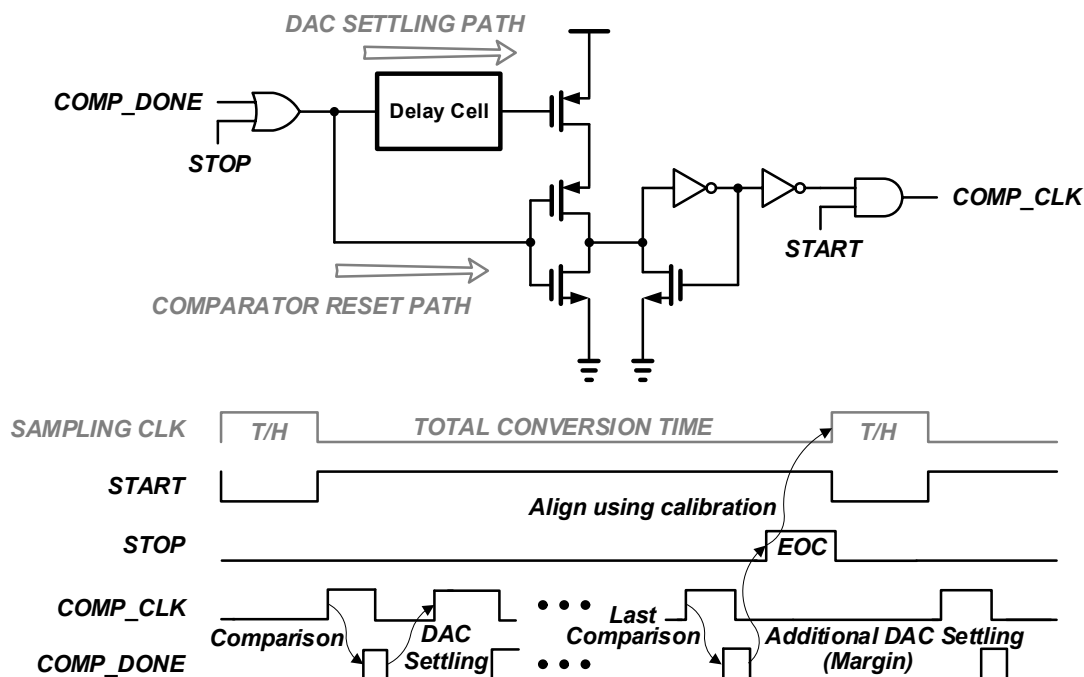


Figure 7. Loop delay circuit of asynchronous SAR ADC.

One feature of the loop delay circuit is that it is divided into the DAC settling path and the comparator reset path depending on the logical state of COMP_DONE. This two path operation has the advantage of using both fast and slow signal passing. However, the internal node of the delay cell can be in undesired states when the low state is applied to the delay cell input, because the input of the delay cell may change before the internal logical states by earlier high state input are entirely

propagated. To prevent these uncertain states in the proposed delay cell, it includes reset switches as shown in Figure 8. The reset switches quickly reset the internal nodes of the delay cell when the comparator reset path is activated. The delay cell is controlled by 5-bit digital input, hence 32 resistors and switches consist of a proposed delay cell. R_{init} , representing the first passive resistance, is replaced by a larger resistance, instead of R , to increase the minimum delay. In addition, a Schmitt trigger is employed at the output stage to prevent any glitch caused by the supply fluctuations [13].

The main drawback of using a passive resistor is that the resistance in the silicon process varies significantly with the process corner or temperature. Particularly, the delay variation is mostly dominated by process variation rather than temperature variation. To resolve this process variation, a foreground calibration is performed for the loop delay circuit. The delay is calibrated so that the STOP indicating the end of the conversion is aligned with the rising edge of next track and hold clock, as shown in Figure 7. Moreover, an additional DAC settling cycle is added to cover the temperature variation, hence securing a 1 cycle margin.

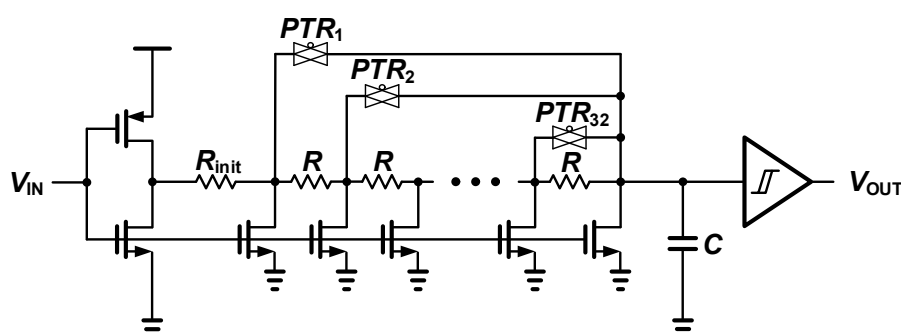


Figure 8. Proposed delay cell circuit including reset switch and Schmitt trigger.

4. Simulation and Measurement Results

Figure 9a shows the calculated delay times from (8) with simulated delays from SPICE simulation according to the input digital codes. In the proposed delay cell, R_{init} and R are $15.1\text{ k}\Omega$ and $1.9\text{ k}\Omega$, respectively, at the nominal corner. $C_{p.off}$ and $C_{p.on}$ are 2.77 fF and 3.45 fF , respectively, and are extracted by the SPICE simulation. Because foreground calibration is performed to correct the delay mismatch from process variation, the delays in all corner conditions meet the 15 ns after calibration. The gray lines show the delays as temperature variations at a nominal corner. Compared to the corner variation, the delay variation from the temperature variation is very small, which is covered by the 1 cycle margin. The calculated delay values reflected the different α values of (3) as the temperature and corner. $R_{on,p}$ and $R_{on,ptr}$ also reflected the temperature and corner variation. Figure 9b shows the step delays from SPICE simulation of the proposed delay cell. The proposed delay cell achieves an error of about 5 percent, owing to the additional 155 fF of Metal-Oxide-Metal (MOM) capacitor C to improve linearity. Figure 10 shows simulation results of best and worst delay errors by component mismatch. From 200 samples of a Monte Carlo simulation, the best and worst delay error are 2.8 percent and 4.4 percent, respectively, with a mean of 3.6 percent and a standard derivation of 0.2 percent. Thus, the effect of mismatch does not significantly affect the delay linearity.

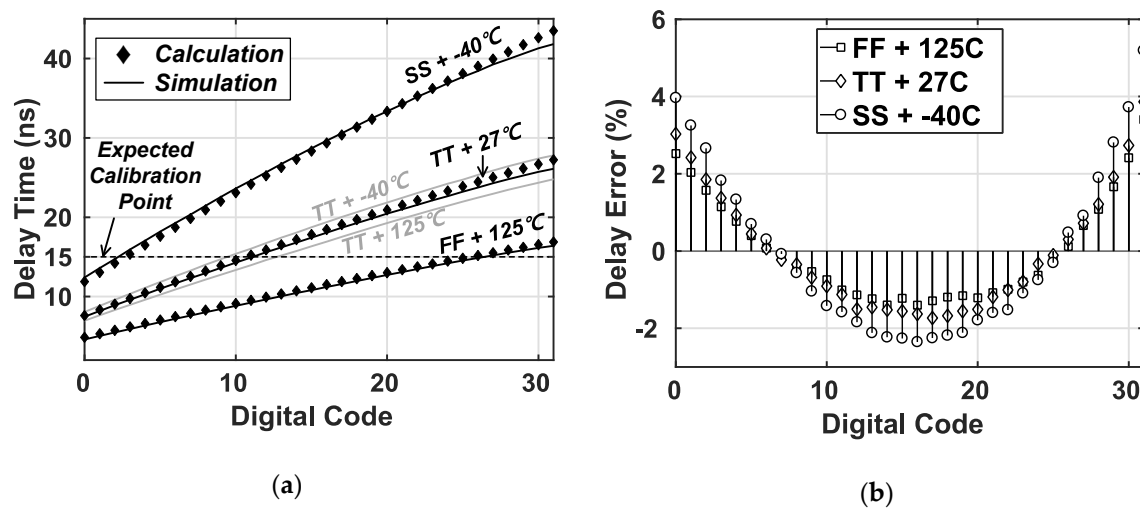


Figure 9. (a) Calculation and SPICE simulation results of delay versus the delay codes; (b) linearity of proposed delay cell from SPICE simulation.

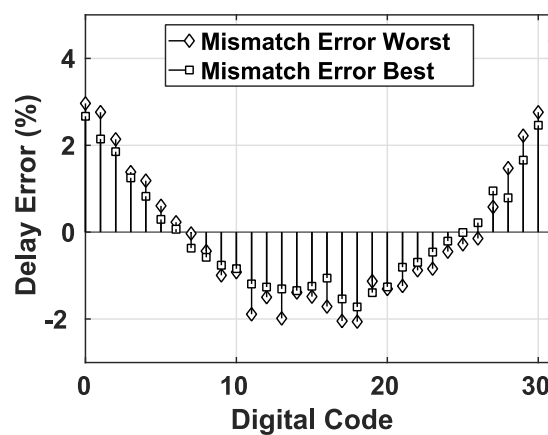


Figure 10. Worst and best linearity of proposed delay cell from Monte Carlo simulation.

Table 1 shows the comparison of delay cell structures with respect to current consumption and delay error. In the case of the current starved delay cell, we followed the design procedure of reference [10] with 30 fF of load capacitor. For fair comparison, the current consumption is measured with clock frequency of 20 MHz, and the each digital codes that adjusts the delay is set to 15ns. In terms of current consumption, the current starved delay cell has low current consumption. However, it has a 45 percent delay error, which is inadequate for tapered bit periods and reconfigurable sampling frequency. Contrarily, the shunt capacitor based delay cell has high linearity but consumes too much current. In case of the passive resistor based delay cell without C , the delay error is 8 percent with same current level of the current starved delay cell. To reduce delay error, the passive capacitor C is added in our application with additional 10 percent of current consumption. In the total power consumption of ADC, the passive resistor based delay cell consumes 28.4 μ W.

Table 1. Comparison of delay cell structure.

Delay Generation Structure	Current (μ A)	Delay Error (%)
Shunt Capacitor [8]	84	4
Current Starved [10]	13.2	45
Passive Resistor with C	14.6	5
Passive Resistor without C	13.2	8

Figure 11 shows the signal to noise and distortion ratio (SNDR) performance of prototype SAR ADC according to the delay codes. As the delay code increases, LSB conversions are not performed due to increased DAC settling delay at a given time, hence degrading SNDR performance. In order to use the proposed delay cell for the ADC with reconfigurable sampling frequency, two frequencies and their corresponding delay codes are required to obtain the relation equation. For example, measuring the sampling frequency of prototype SAR ADC at 2 MHz and 3 MHz from two delay calibrations, the corresponding delay codes from calibration are 0 and 11, respectively. Then, in the case of 2.5 MHz, the calculated delay code is 5.5 from the relation equation made with a two point calibration, and thus, delay code of 5 is applied, which is well matched to the measurement at a 2.5 MHz sampling frequency. The delay codes where the bits are skipped also show that the delay cell is sufficiently linear to be utilized for the ADC with a varied sampling frequency.

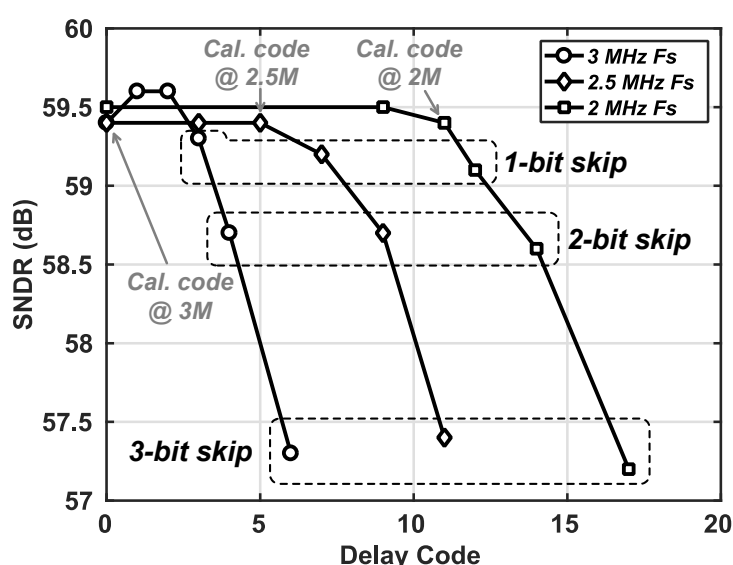


Figure 11. SNDR performance of SAR ADC as delay codes.

The prototype SAR ADC is fabricated in the 40 nm CMOS process. Figure 12 shows the die photograph of prototype SAR ADC, which occupies a core area measuring $670\text{ }\mu\text{m} \times 80\text{ }\mu\text{m}$. The delay cell occupies $35\text{ }\mu\text{m} \times 17\text{ }\mu\text{m}$, which is about 1 percent of total area. The prototype SAR ADC operates under 1.1 V supply voltage, consuming $67\text{ }\mu\text{W}$ at the 3 MHz sampling frequency. Figure 13 shows the differential nonlinearity (DNL) and integral nonlinearity (INL). The peak DNL are 2.9/-1 LSB, and the peak INL are 5.8/-10.5 LSB. Figure 14 shows an output spectrum from the prototype SAR ADC for near 100 kHz and 1.5 MHz. With a near 100 kHz input frequency, a measured spurious free dynamic range (SFDR) and SNDR are 68 dB and 59.4 dB, respectively. With a near 1.5 MHz input frequency, the prototype ADC achieves an SFDR of 65.2 dB and SNDR of 57.4 dB, yielding a FoM of 35.4 fJ/conversion-step. The overall performance of the prototype ADC is summarized in Table 2 and compared to references [14–17].

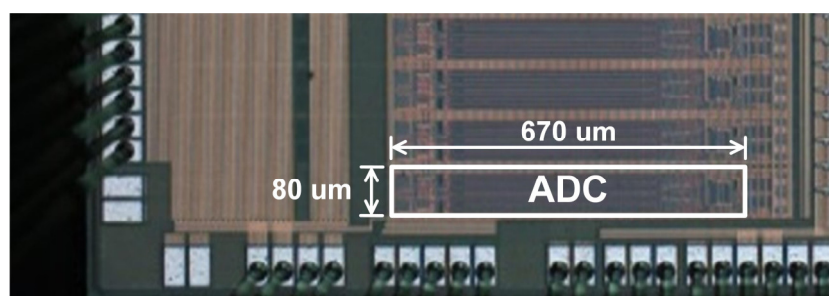


Figure 12. Die photograph.

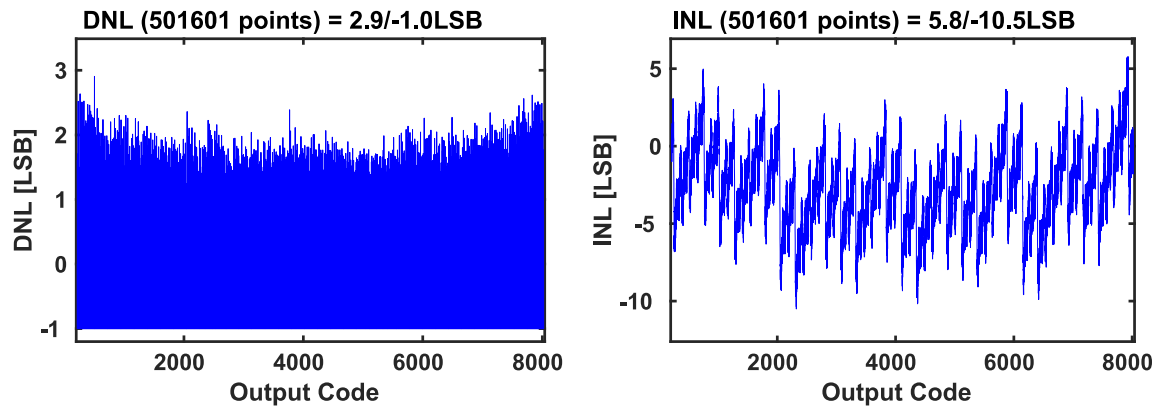


Figure 13. Static performance of prototype SAR ADC.

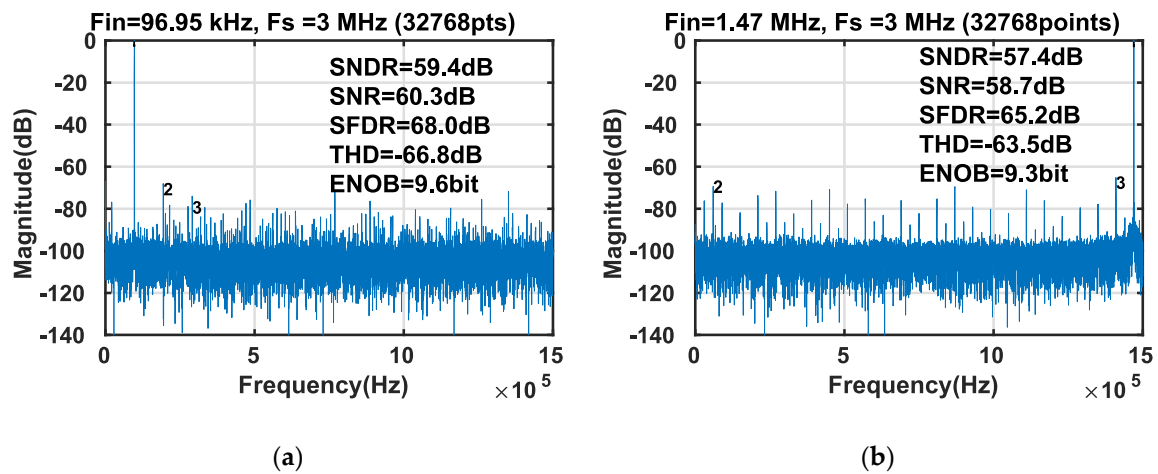


Figure 14. Measured output spectrum of prototype SAR ADC with (a) a near 100 kHz sinusoidal input; (b) a near 1.5 MHz sinusoidal input.

Table 2. Performance summary and comparison.

Reference	[14]	[15]	[16]	[17]	This work
Technology (nm)	110	180	180	28	40
Resolution (bit)	10	10	12	12	13
Supply Voltage (V)	1.2	0.9	1.8	1	1.1
Sampling Rate (MS/s)	10	2	10	4	3
ENOB (bit)	8.6	9.07	10.82	10.1	9.3
FoM (fj/conversion-step)	409	20.6	44.2	26	35.4
Power (μ W)	1640	22.12	820	115	67
Area (mm ²)	0.25	0.21	0.359	0.016	0.054

5. Conclusion

In this paper, a 13 bit 3 MS/s asynchronous SAR ADC with a passive resistor based delay cell is presented. The proposed delay cell adopts passive resistors, which yields a delay error of less than 5 percent with reduced power consumption. The prototype SAR ADC achieves 57.4 dB of SNDR with 67 μ W power dissipation, which converts to FoM of 35.4 fj/conversion-step. This measurement shows that the scaling of delay codes can cope with the reconfigurable sampling frequency.

Author Contributions: Conceptualization, H.J.; Data curation, H.J.; Formal analysis, H.J.; Funding acquisition, M.L.; Investigation, H.J.; Methodology, H.J.; Project administration, M.L.; Supervision, M.L.; Visualization, H.J.; Writing – original draft, H.J.; Writing – review & editing, H.J.

Funding: This research was supported by the National Research Foundation of Korea Grant funded by the Korean Government (NRF-2016R1A2B4016544). The EDA tools were supported by IDEC, Korea.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Koppa, S.; Mohandesi, M.; John, E. An ultra-low power charge redistribution successive approximation register A/D converter for biomedical applications. *J. Low Power Electron.* **2016**, *12*, 385–393.
2. Bai, W.; Zhu, Z. A 0.5-V 9.3-ENOB 68-nW 10-kS/s SAR ADC in 0.18- μ m CMOS for biomedical applications. *Microelectron. J.* **2017**, *59*, 40–46.
3. Fan, H.; Heidari, H.; Maloberti, F.; Li, D.; Hu, D.; Cen, Y. High resolution and linearity enhanced SAR ADC for wearable sensing systems. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), Baltimore, MD, USA, 28–31 May 2017, pp. 1–4.
4. Frans, Y.; Shin, J.; Zhou, L.; Upadhyaya, P.; Im, J.; Kireev, V.; Borrelli, C. A 56-Gb/s PAM4 wireline transceiver using a 32-way time-interleaved SAR ADC in 16-nm FinFET. *IEEE J. Solid-State Circuits* **2017**, *52*, 1101–1110.
5. Aryanfar, F.; Hossain, M. A quad channel 11-bit 1 GS/s 40 mW Collaborative ADC based enabling digital beamforming for 5G wireless. In the Proceedings of the IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Honolulu, HI, USA, 4–6 June 2017, pp. 120–123.
6. Shen, Y.; Zhu, Z.; Liu, S.; Yang, Y. A Reconfigurable 10-to-12-b 80-to-20-MS/s Bandwidth Scalable SAR ADC. *IEEE Trans. Circuits Syst. Regul. Pap.* **2018**, *65*, 51–60.
7. Janke, D.; Monk, A.; Swindlehurst, E.; Layton, K.; Chiang, S. H. W. A 9-Bit 10-MHz 28- μ W SAR ADC using Tapered Bit Periods and a Partially Interdigitated DAC. *IEEE Trans. Circuits Syst. Express Briefs* **2018**, *66*, 187–191.
8. Ramazanoglu, S.; Batur, O.Z. Switched Capacitor Variable Delay Line. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, 27–30 May 2018, pp. 1–5.
9. Saint-Laurent, M.; Swaminathan, M. A digitally adjustable resistor for path delay characterization in high-frequency microprocessors. In Proceedings of the IEEE Southwest Symposium on Mixed-Signal Design (SSMSD), Austin, TX, USA, 25–27 February 2001, pp. 61–64.
10. Maymandi-Nejad, M.; Sachdev, M. A digitally programmable delay element: design and analysis. *IEEE Trans. Very Large Scale Integr. VLSI Syst.* **2003**, *11*, 871–878.
11. Yang, R.J.; Liu, S.I. A 40–550 MHz harmonic-free all-digital delay-locked loop using a variable SAR algorithm. *IEEE J. Solid-State Circuits* **2007**, *42*, 361–373.
12. Weste, N.H.; Harris, D. *CMOS VLSI design: a circuits and systems perspective*. Pearson Education: Chennai, India, 2015.
13. Melek, L.A.P.; da Silva, A.L.; Schneider, M.C.; Galup-Montoro, C. Analysis and design of the classical CMOS Schmitt trigger in subthreshold operation. *IEEE Trans. Circuits Syst. Regul. Pap.* **2017**, *64*, 869–878.
14. Nam, S. P.; Kim, Y. M.; Hwang, D. H.; Kim, H. J.; An, T. J.; Park, J. S.; Lee, S. H. A 10b 1MS/s-to-10MS/s 0.11 μ m CMOS SAR ADC for analog TV applications. In Proceedings of the IEEE International SoC Design Conference (ISOCC), Jeju, Korea, 4–7 November 2012, pp. 124–127.
15. Zhu, Z.; Qiu, Z.; Liu, M.; Ding, R. A 6-to-10-Bit 0.5 V-to-0.9 V Reconfigurable 2 MS/s Power Scalable SAR ADC in 0.18 μ m CMOS. *IEEE Trans. Circuits Syst. Regul. Pap.* **2015**, *62*, 689–696.
16. Liu, S.; Shen, Y.; Zhu, Z. A 12-bit 10 MS/s SAR ADC with high linearity and energy-efficient switching. *IEEE Trans. Circuits Syst. Regul. Pap.* **2016**, *63*, 1616–1627.
17. Haenzsche, S.; Höppner, S.; Ellguth, G.; Schüffny, R. A 12 bit 4 MS/s SAR ADC with configurable redundancy in 28 nm CMOS technology. *IEEE Trans. Circuits Syst. Express Briefs* **2014**, *61*, 835–839.

