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A design of a 5.6 GHz frequency synthesizer with switched bias LIT VCO and low noise on-chip LDO regulator for 5G applications

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delta-sigma modulator, frequency synthesizer, linear transconductance, low-noise LDO, switched bias

1 | INTRODUCTION

The frequency band of 4G is becoming saturated, and the demand for faster communication speed has made research into 5G communication technology increasingly essential. Phase noise is one of the most important parameters in the design of high-speed radio frequency (RF) transceivers. If the phase noise performance is not good, the error vector magnitude (EVM) performance cannot be satisfied. Various methods for improving the phase noise performance of fractional-N frequency synthesizers in the 3/4G standard have been published in previous papers.[1-15] The block that exerts the greatest influence on the phase noise performance over the frequency synthesizer is the voltage controlled oscillator (VCO). A method for remarkably improving the phase noise of the VCO is presented in Lee et al.[2] In addition, Siriburanon et al[3] proposed a low-phase noise frequency synthesizer using subsampling technique.

In order to perform complex modulation schemes in 5G cellular networks, both the in-band and out-of-band phase noises should be as low as possible.[1] In a frequency synthesizer, the phase noise is divided into in-band phase noise and out-of-band phase noise. The phase frequency detector (PFD) and charge pump (CP) noise dominate the in-band-phase noise. The noise of the PFD and CP is multiplied by N, where N is the division ratio in the feedback loop. In addition, the quantization noise of the delta-sigma modulator (DSM) is sensitive to the current mismatch of the CP, resulting in poor in-band phase noise. Furthermore, the out-of-band phase noise is significantly affected by the VCO phase noise and DSM noise.[1]

The noise characteristic of the VCO is greatly affected by the noise of the power supply to the VCO. Therefore, the noise characteristics of the power supply circuit are very important.[4]

In this work, we propose a low phase noise 5.6 GHz frequency synthesizer with a switched bias linear transconductance VCO (SBLIT-VCO) and a low noise on-chip regulator for 5G applications. In order to minimize the noise generated by the CP, a loop filter switch (LF_SW) was added so as to improve the in-band phase noise. For low out-of-band phase noise performance, SBLIT_VCO is proposed. A multi-stage noise shaping (MASH) 1-1-1 DSM is designed, and the reference clock doubler is used to reduce the out-of-band phase noise. In order to not degrade the phase noise of VCO, a low-noise low drop out (LN_LDO) is designed as well. Figure 1 shows the spectrum of the

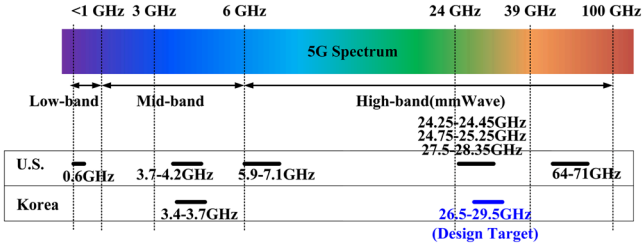

FIGURE 1 Frequency band of 5G system [Colour figure can be viewed at wileyonlinelibrary.com]

5G frequency band in the US and Korea. There are both mid-band and high-band frequencies in Korea. To support high-band frequency, the proposed frequency synthesizer uses the structure shown in Figure 2, which is a block diagram of a dual-conversion receiver composed of two stages of mixer. The proposed frequency synthesizer supplies 20 to 24 GHz and 5 to 6 GHz frequencies to the first stage LO and the second stage LO, respectively.

The rest of this paper is organized as follows. Section 2 details the overall structure of the frequency synthesizer to implement the proposed low noise. Section 3 describes each block in detail. Section 4 describes the frequency synthesizer implementation in detail as well as the verification of the actual measurements. The final section, Section 5, concludes with the design of the proposed low noise frequency synthesizer.

2 | FREQUENCY SYNTHESIZER

2.1 | Architecture

The architecture of the 5.6-GHz frequency synthesizer is shown in Figure 3. It consists of a 5.6-GHz SBLIT-VCO with automatic frequency calibration (AFC), digital automatic amplitude calibration (AAC), divider-4, fractional-N divider with MASH 1–1-1 DSM, PFD, CP, LF_SW, a three-order loop filter (LF), and LN_LDO. Since the frequency tuning range of the VCO is 5.23 to 6.09 GHz, it can cover the 5.3 to 5.9 GHz range, as required by the specification. The channel spacing of the frequency bands and reference clock are 10.62 MHz and 54 MHz, respectively. The reference clock doubler increases the sampling clock and over sampling ratio (OSR) of the DSM, and this can improve the noise shaping

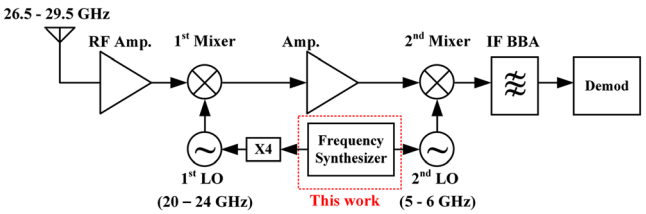

FIGURE 2 Block diagram of double-conversion receiver of 5G applications [Colour figure can be viewed at wileyonlinelibrary.com]

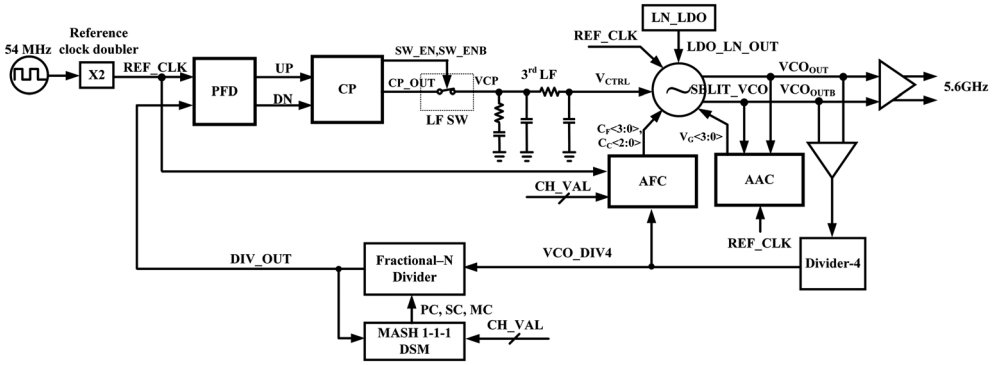

FIGURE 3 Block diagram of the proposed frequency synthesizer

characteristics of the DSM and phase noise. It can also improve the in-band phase noise by decreasing the fractional division ratio (N).

In order to cover the frequency band of 5.3 to 5.9 GHz, the VCO is composed of a coarse tuning capacitor bank (C_C<2:0>), fine tuning capacitor bank (C_F<3:0>), and varactor. The AFC block makes decisions on the optimal coarse tuning capacitances through the 7-bit control signals of C_C<2:0> and C_F<3:0>. Therefore, the AAC block has the advantage of allowing the output amplitude of the SBLIT-VCO to be kept constant regardless of the frequency and the PVT variation of the VCO.

Figure 4 shows the contribution of the frequency synthesizer with LDO noise to the phase noise. The total noise of the frequency synthesizer is the sum of each block noise, and the noise of the LDO contributes to the in-band phase noise. This paper stresses the importance of the low-frequency noise synthesizer's low phase noise performance as well as the noise relation of LDO.

3 | BULDING BLOCKS

3.1 | Switched bias linear transconductance VCO

Figure 5 shows a schematic of the SBLIT-VCO. The linear transconductance VCO (LIT-VCO) has a higher voltage swing and lower phase noise performance than the basic cross-coupled VCO structures,[2] making it suitable for low-phase noise applications. In this work, we apply the switched bias technique so as to further improve the phase noise in the LIT-VCO. The flicker noise of V_G.bias can be up-converted to the frequency of the VCO, and the performance of the phase noise is degraded by the flicker noise. Therefore, the flicker noise of the bias voltage is removed using the switched capacitor filter method.[4] The 3-dB cutoff frequency (f-3 dB) of the switched-capacitor filter is defined as Equation (1).

$$f_{-3dB} = \frac{1}{2\pi} CLK_{SW} \times \frac{C_{s1}}{C_{s2}} \tag{1}$$

Figure 6A,B show a block diagram and timing diagram of AAC. The AAC block consists of a peak detector, a REF_GEN, a comparator, and a digital controller as shown in Figure 6A. Figure 4B shows the timing diagram of the AAC block. The AAC block operates in synchronization with REF_CLK. The peak detector converts the output of the VCO to a DC voltage and compares this voltage to the VREF voltage, which is the output voltage of REF_GEN.

If the PEAK_A voltage is less than the VREF voltage during AAC operation, the VG<3:0> value is automatically adjusted so as to control the swing of the VCO. Therefore, the AAC block keeps the amplitude of the VCO constant, regardless of any PVT variations.[3]

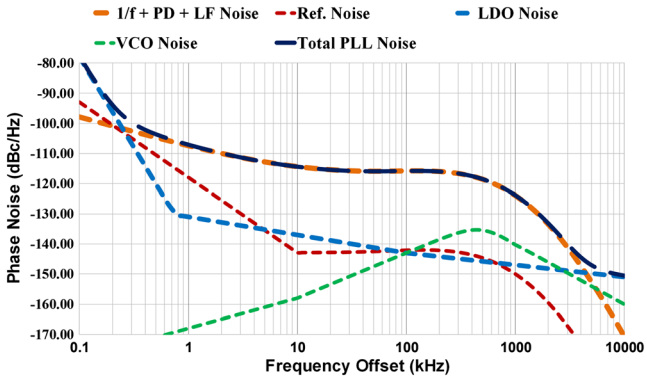

FIGURE 4 Contribution of building blocks of frequency synthesizer to the phase noise

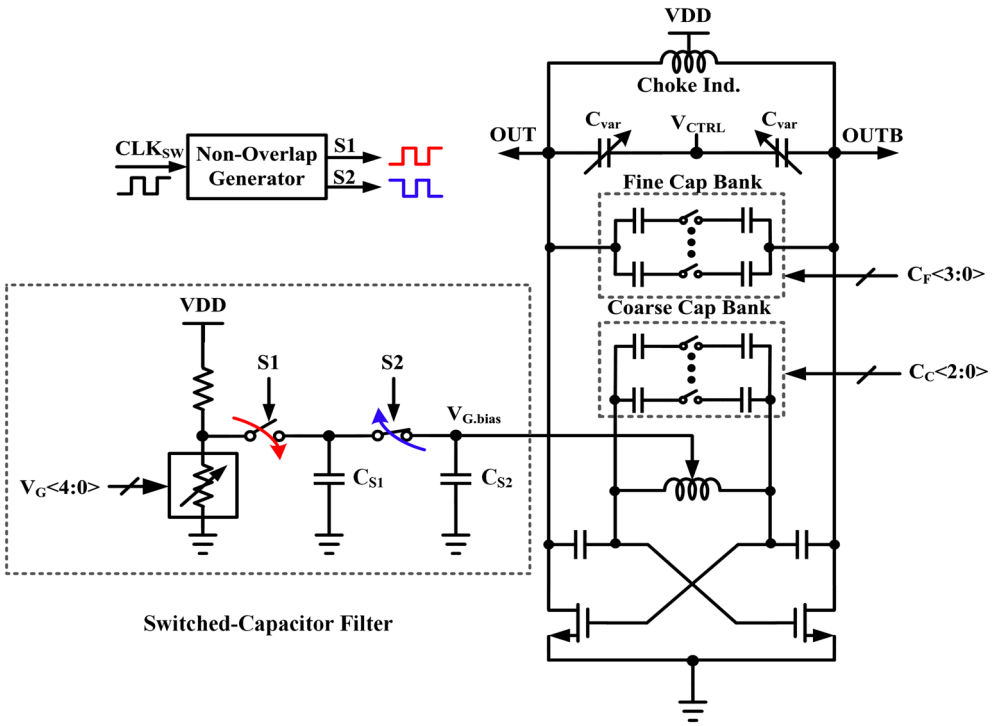

FIGURE 5 Switched bias linear transconductance voltage controlled oscillator (SBLIT-VCO) schematic [Colour figure can be viewed at wileyonlinelibrary.com]

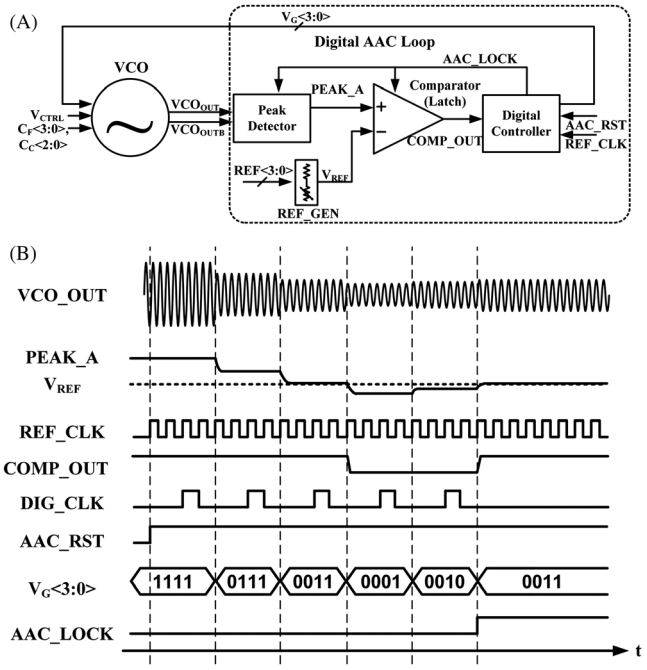

FIGURE 6 (A) Block diagram and (B) timing diagram voltage-controlled oscillator (VCO) with automatic amplitude calibrator (AAC) block

3.2 | Reference clock doubler

In general, in order to provide precise carrier frequencies, a fractional-N frequency synthesizer is implemented using a DSM. However, using a DSM is disadvantageous in that it encounters the noise and fractional spur of the DSM. If these

noise components are located near the in-band of the frequency synthesizer, the phase noise of the frequency synthesizer is degraded and thus does not satisfy the integrated phase noise (IPN) performance. In addition, when the reference clock is low, the division ratio of the frequency synthesizer increases, which causes the noise generated by the PFD and CP to increase. Therefore, a fractional-N frequency synthesizer using a high reference clock frequency is preferred. The reference clock doubler consists of a buffer delay chain and an XOR gate, as shown in Figure 7A. Figure 5B shows the timing diagram of a reference clock doubler. It generates a REF_CLK signal, which is twice the frequency of 54 MHz, using a 54 MHz signal and phase delayed T/4 signal.

3.3 | Charge pump and loop filter switch

A schematic of the CP and LF_SW is shown in Figure 8. The in-band phase is affected by the reset delay of UP/DN. However, the proposed loop LF_SW can decrease this reset delay. If the UP/DN signals are simultaneously high, the LF_SW shown in Figure 9 is turned off. Therefore, the variation of the V_{CP} is decreased because the I_{CP} cannot pass to the loop filter during the reset delay. The noise caused by the reset delay can be decreased. Figure 10 shows the simulation results of the LF_SW. When the LF_SW is not applied, the glitch current is 1.8 mA. The glitch peak current can be reduced to 0.45 mA when the LF_SW is applied.

3.4 | Delta-sigma modulator

For the fractional-N frequency synthesizer, the fractional spurs are reduced through using of the DSM. It can apply a technique that can randomly change the dividing factor (PC, SC, and MC) of the fractional-N divider. Figures 11A and 9B show two types of schematics of the DSM. The device consists of a full-adder, register, and CH_MAP. The CH_MAP seen in Figure 3 calculates the values of the DSM_I, PC, SC, and MC by CH_VAL, which is defined for

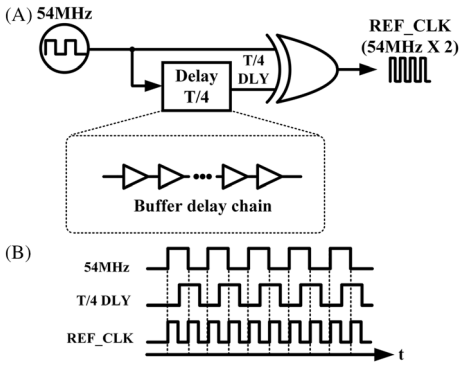

FIGURE 7 (A) Block diagram of reference clock doubler and (B) timing diagram of reference clock doubler

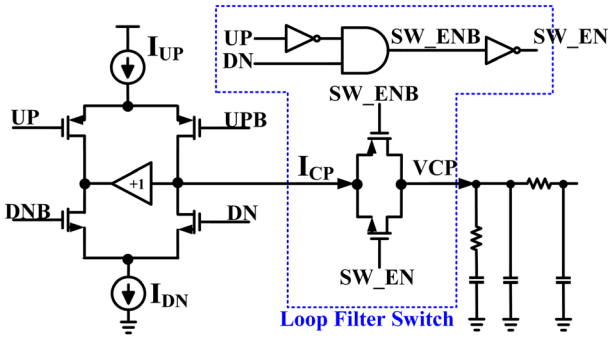

FIGURE 8 The charge pump (CP) and loop filter switch (LF_SW) schematic [Colour figure can be viewed at wileyonlinelibrary.com]

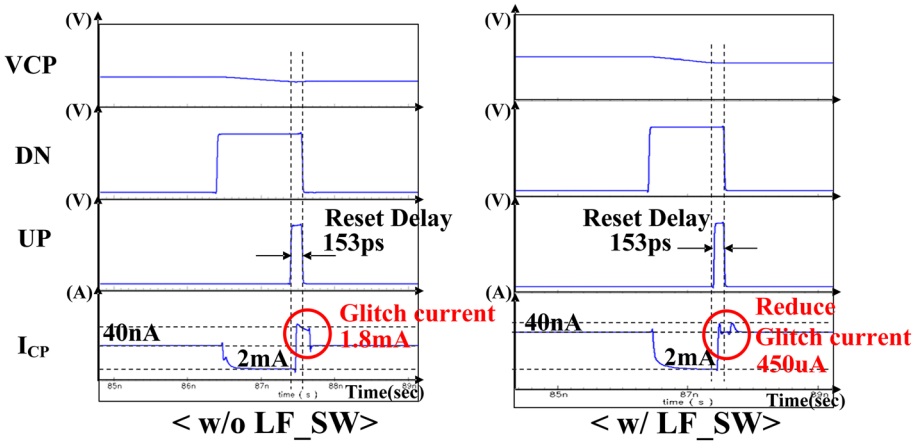

FIGURE 9 Charge pump (CP) current simulation result of without and with loop filter switch (LF_SW) [Colour figure can be viewed at wileyonlinelibrary.com]

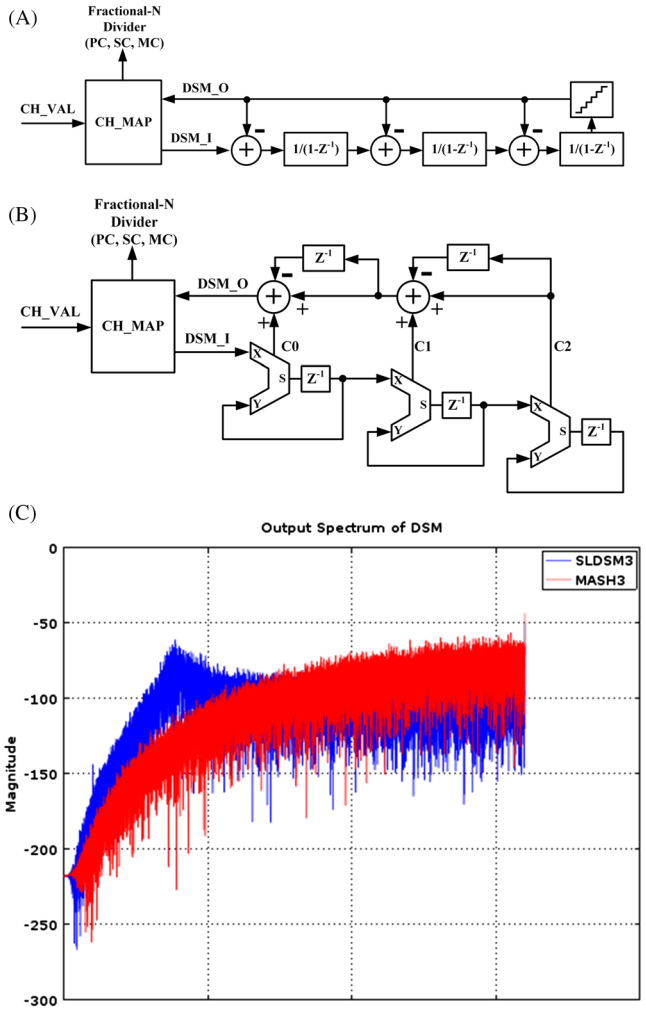

FIGURE 10 (A) Block diagram of single loop delta-sigma modulator (SLDSM), (B) multi-stage noise shaping (MASH) 1-1-1 DSM, and (c) comparison of the SLDSM and MASH 1-1-1 DSM output spectrum [Colour figure can be viewed at wileyonlinelibrary.com]

the desired frequency. The quantization noise transfer functions of single loop DSM (SLDSM) and MASH 1-1-1 DSM are described as Equations (2) and (3), respectively.

$$Y_{SLDSM}(z) = \mathrm{X}(\mathrm{z})\cdot z^{-1} + Q(z)\cdot\left(1-\mathrm{z}^{-1}\right)^{3} \tag{2}$$

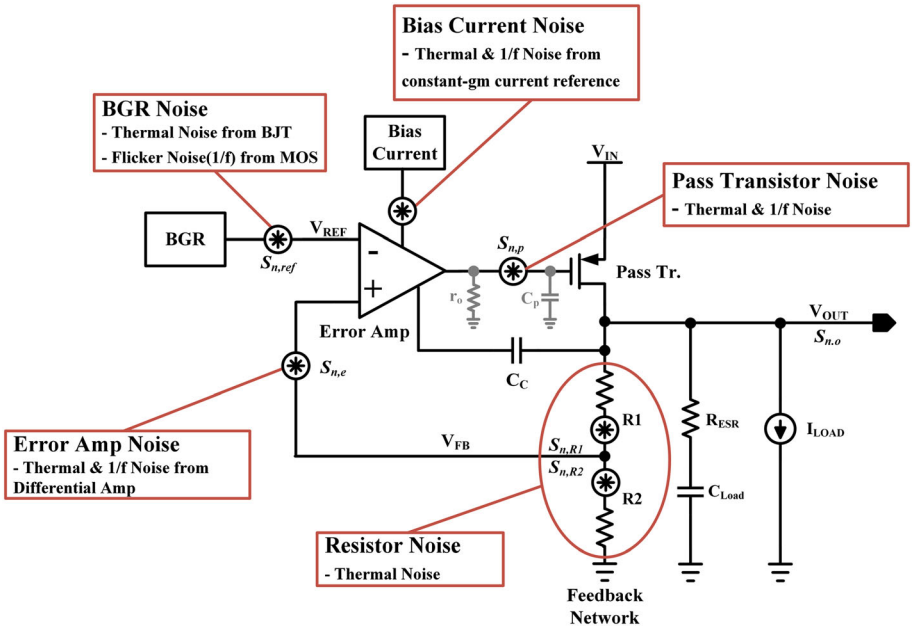

FIGURE 11 Noise sources of conventional low drop-out (LDO) regulator [Colour figure can be viewed at wileyonlinelibrary.com]

$$Y_{MASH1-1-1}(z) = \mathrm{X(z)}\cdot z^{-3} + Q(z)\cdot\left(1-\mathrm{z}^{-1}\right)^3 \tag{3}$$

Using Equations (2) and (3), the noise of SLDSM and MASH 1-1-1 can be compared by simulation. Figure 12C shows the simulation result of the spectrum of SLDSM and MASH 1-1-1 DSM. At a low frequency, the MASH type has a lower noise level than the single loop.[16]

3.5 | Low-noise LDO

Figure 11 shows the noise source of LDO. It is analyzed in order to determine the dominant part of the noise sources. In the proposed LN_LDO, in order to reduce the noise of the LDO regulator, a low-pass filter is added between the bandgap reference (BGR) and the input of the error amplifier of the LDO.

A schematic of the LN_LDO is shown in Figure 12. The sensitivity of the power supply noise should be decreased in order to achieve the wideband and low-phase noise performances of VCO. Therefore, the LDO is recommended for insensitive power supply noise. However, the LDO with the low noise should be required because the output noise of the LDO affects the phase noise.

The variation of the VCO output frequency with respect to the change of the power supply voltage is defined as K_{PUSH}, and is generally about 5% to 20% of the K_{VCO}. The noise of LDO, taking into account the effects of K_{PUSH}, can be calculated as Equations (4).

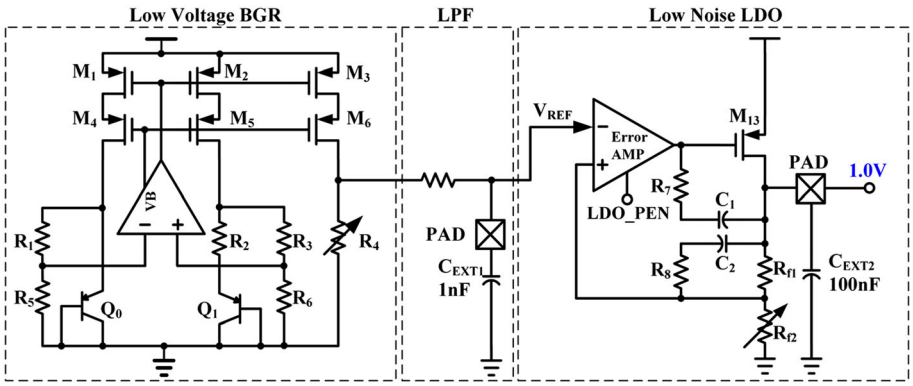

FIGURE 12 Schematic of low-noise low drop-out (LN_LDO) [Colour figure can be viewed at wileyonlinelibrary.com]

$$\begin{aligned}\Phi_{\mathrm{LDO}}(\mathrm{t}) &= \mathrm{K}_{\mathrm{PUSH}}\cdot\int V_{\mathrm{LDO}}(\mathrm{t})\mathrm{dt}\\ \Phi_{\mathrm{LDO}}(\mathrm{f}) &= \frac{K_{\mathrm{PUSH}}\cdot V_{\mathrm{LDO}}(f)}{f}\\ L_{\mathrm{LDO}} &= 10\log\left(\frac{K_{\mathrm{PUSH}}\cdot {V_{\mathrm{LDO}}}^2}{2f^2}\right)\\ L_{\mathrm{LDO}} &= 20\log\left(\frac{K_{\mathrm{PUSH}}\cdot V_{\mathrm{LDO}}}{\sqrt{2}\cdot f}\right).\end{aligned} \tag{4}$$

In the free-running VCO, the total noise (L_{total}) is the LDO noise (L_{LDO}) and the VCO noise (L_{VCO}). Thus, expressed in dB

$$\begin{aligned}L_{\mathrm{total}} &= \sqrt{{L_{\mathrm{VCO}}}^2 + {L_{\mathrm{LDO}}}^2}\\ L_{\mathrm{total}} &= 10\log\left[10^{\frac{L_{\mathrm{VCO}}}{10}} + 10^{\frac{L_{\mathrm{LDO}}}{10}}\right].\end{aligned} \tag{5}$$

Therefore, in order to prevent deterioration of VCO noise, LDO noise should be designed to be at least 6 dB, and the relationship between the LDO noise specifications and the K_{PUSH} specifications of VCO from Equations (4) is required as Equations (6).

$$V_{\mathrm{LDO}}(f) = 10^{\frac{L_{\mathrm{LDO}}}{20}}\cdot\frac{\sqrt{2}\cdot f}{K_{\mathrm{PUSH}}}, \tag{6}$$

where, f and $V_{\mathrm{LDO}}(f)$ are the frequency offsets from the carrier frequency in Hz, and the noise spectral density at a given frequency offsets in V/$\sqrt{\mathrm{Hz}}$, respectively.

Assuming that K_{PUSH} is 60 MHz/V, the noise specification of the LDO is derived based on Equations (4) to (7) and summarized in Table 1.

TABLE 1 Noise specification of LDO

Offset frequency, kHz	Noise, V^2/Hz
10	2.0e-15
100	1.4e-15
1000	1.0e-16

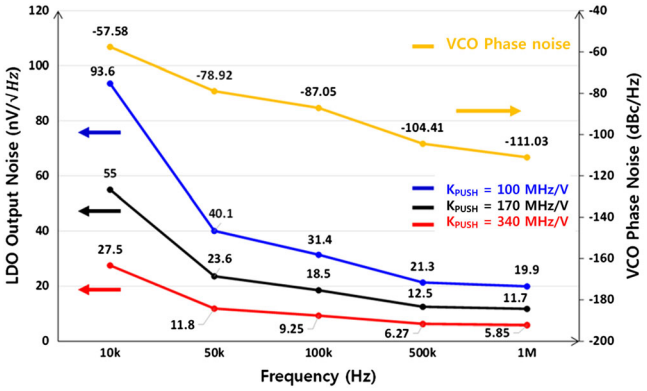

FIGURE 13 Relationship between output noise of low drop-out (LDO) regulator and phase noise of voltage-controlled oscillator (VCO) [Colour figure can be viewed at wileyonlinelibrary.com]

$$V_{LDO}(1MHz) = 10^{\frac{-128}{20}} \times \frac{\sqrt{2} \times 1MHz}{60MHz/V} = 10nV/\sqrt{Hz}. \quad (7)$$

The output noise characteristics of the LDO regulator should be determined by analyzing the phase noise of the VCO and the rate of change of frequency because of the VCO power variation.

Figure 13 shows the LDO output noise specification according to K_{PUSH} and VCO phase noise. For example, if the K_{PUSH} increases from 170 to 340 MHz/V, the output noise specification of the LDO at 10 kHz offset frequency must be reduced to one-half (27.5 nV/$\sqrt{}$Hz) in order to obtain the same VCO phase noise specification and thus maintain the same phase noise performance. Therefore, as the K_{PUSH} of the VCO increases, the LDO output noise must be small in order to satisfy the VCO phase noise specification.

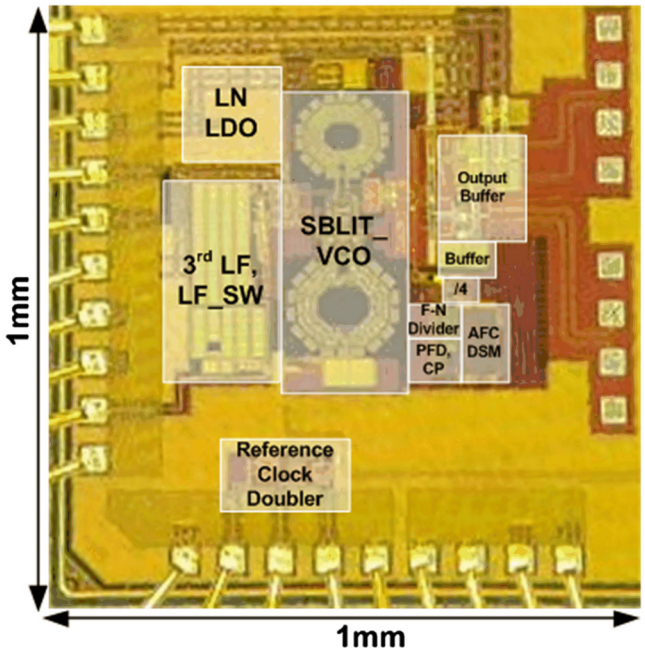

FIGURE 14 Chip microphotograph of proposed frequency synthesizer with PADs [Colour figure can be viewed at wileyonlinelibrary.com]

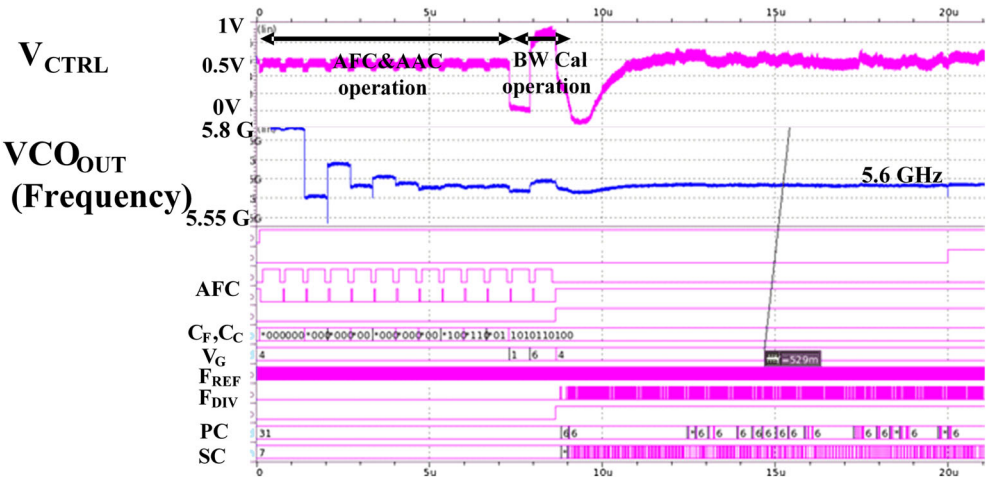

FIGURE 15 . Transient simulation result of proposed frequency synthesizer [Colour figure can be viewed at wileyonlinelibrary.com]

4 | EXPERIMENTAL RESULTS

Figure 14 shows the chip microphotograph of the frequency synthesizer fabricated using a 65-nm CMOS. The die area including the ESD PADs is 1 mm^2.

Figure 15 shows the top simulation results of the proposed frequency synthesizer. The frequency synthesizer locks to 5.585 GHz after the sequential process of AFC, AAC, and BW calibration.

The measured output spectrum of the proposed frequency synthesizer is shown in Figure 14. The measured tuning range of the proposed frequency synthesizer is from 5.3402 to 5.8298 GHz. In addition, the output power levels of the frequency synthesizer consistently show results between −5.6 and −5.5 dBm in the frequency band Figure 16.

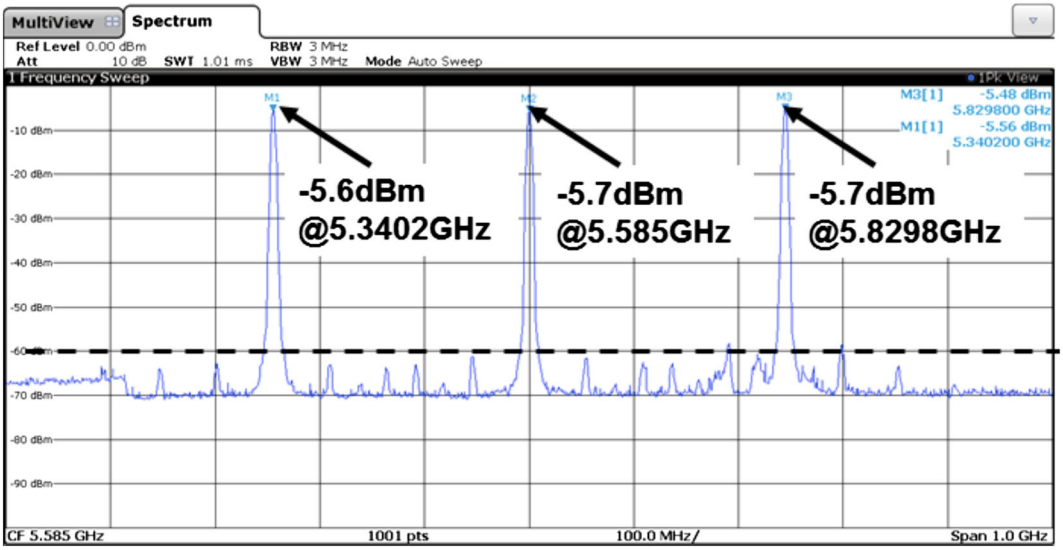

FIGURE 16 . Output spectrum of frequency synthesizer [Colour figure can be viewed at wileyonlinelibrary.com]

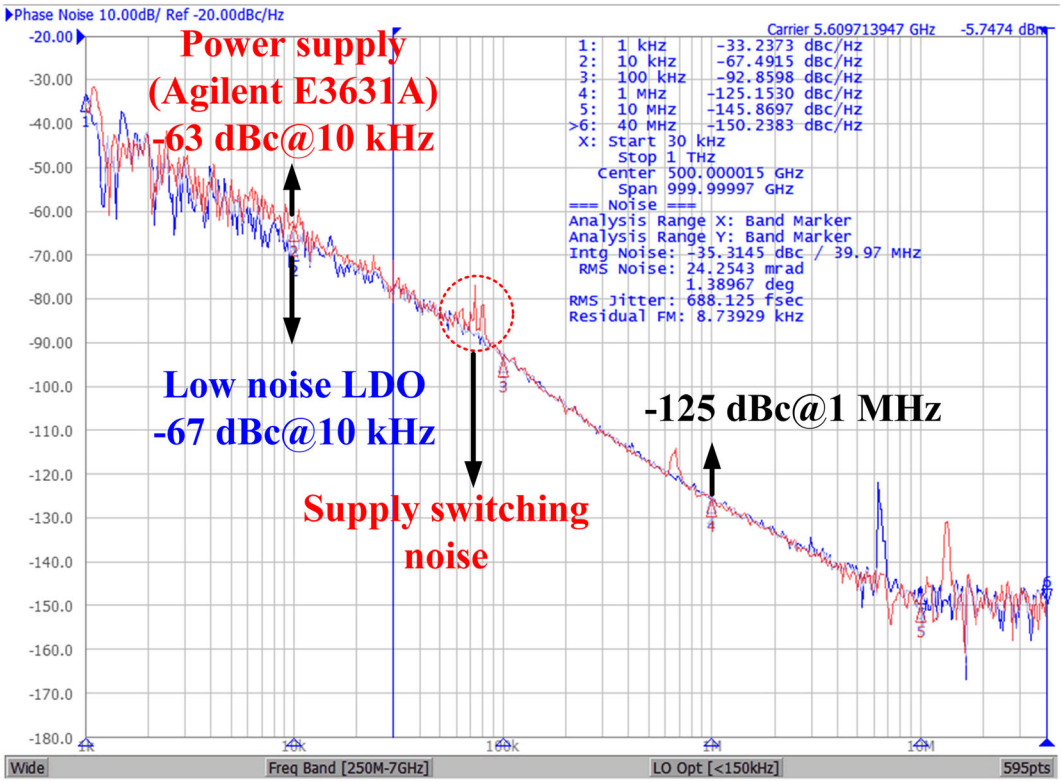

FIGURE 17 Comparison of voltage-controlled oscillator (VCO) phase noise with low-noise low drop-out (LDO) [Colour figure can be viewed at wileyonlinelibrary.com]

Figure 17 shows the measured phase noise of the open loop VCO output. When the Agilent E3631A is used as the power supply without the proposed LDO, the performance of the phase noise is −63 dBc/Hz at the 10 kHz offset. However, the performance of the phase noise is improved by around 4 dB when using the proposed LN_LDO. The supply switching noise can be removed as well.

Figure 18 shows the measured phase noise of the frequency synthesizer with and without the LF_SW in the closed loop. The phase noise performances with and without the LF_SW are −86 and −83 dBc/Hz, respectively, at an offset frequency of 10 kHz. This result indicates that the LF_SW helps improve the in-band phase noise.

Figure 18 shows the measured output noise of the LN_ LDO. The measured noises are 3.397e-15, 1.120e-15, and 4.754e-19 V^2/Hz at 10, 100, and 1 MHz, respectively (Figure 19).

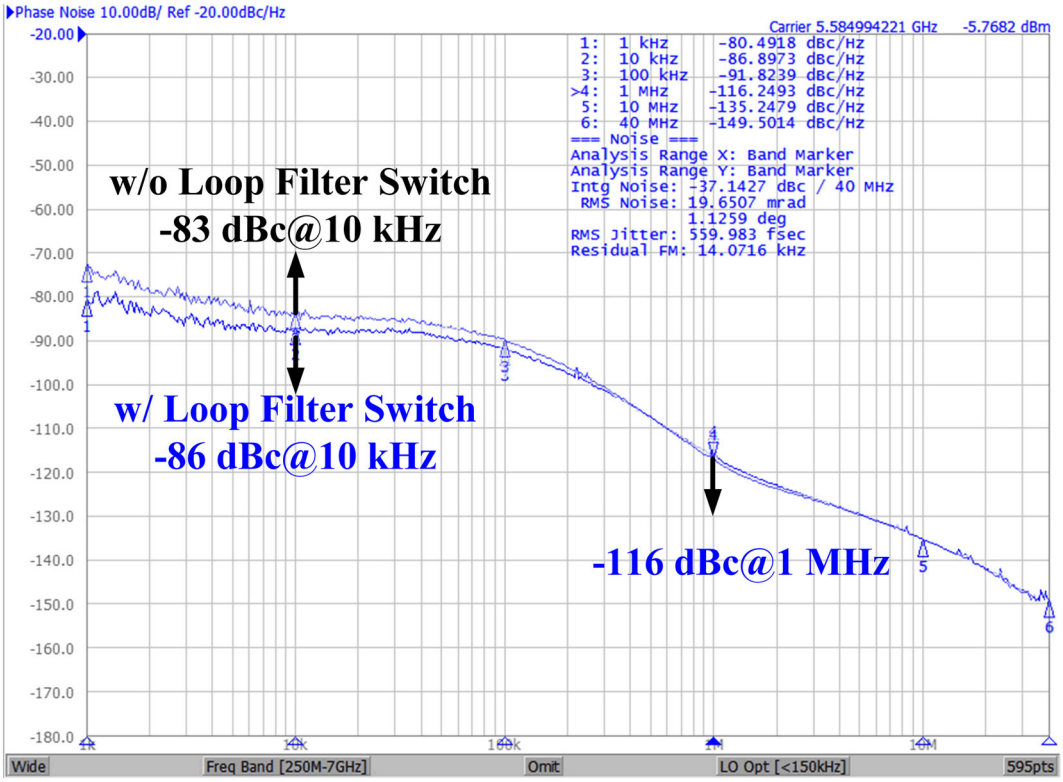

FIGURE 18 Comparison of frequency synthesizer phase noise when using loop filter switch (LF_SW) [Colour figure can be viewed at wileyonlinelibrary.com]

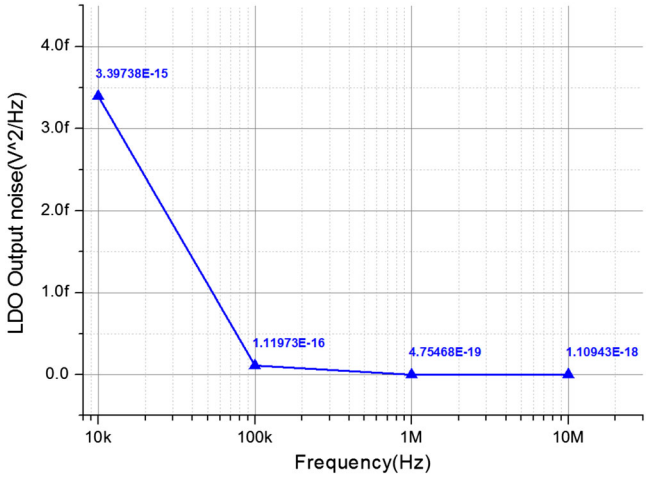

FIGURE 19 Measured output noise of low noise low drop-out (LN_LDO) [Colour figure can be viewed at wileyonlinelibrary.com]

Figure 20 shows the measured PSRR of the LN_LDO. The PSRR of the proposed LDO with a 4.7-μF output capacitor is measured using E5061B in the range from 100 Hz to 10 MHz when the output load current is 25 mA. The PSRR of LN_LDO is better than −33 dB, and the best PSRR performance is achieved below −100 dB at up to 200 Hz.

Table 2 compares the proposed 5.6-GHz frequency synthesizer performance with those of the other frequency synthesizers designed for 5.6 GHz applications. When compared with the performances described in other papers,[8-10] the proposed frequency synthesizer has the lowest phase noise of −117 dBc/Hz at a 1 MHz offset from its center frequency, 5.585 GHz, the lowest power consumption of 24 mW and the best FOM_{PLL} of −178.14 dBc/Hz.

The FOM_{PLL} is defined as Equation (7).

$$FOM_{PLL} = L(\Delta\omega) - 20\cdot\log(\omega_0/\Delta\omega) + 10\cdot\log(P_{diss}/1\text{mW}), \tag{7}$$

where, ω_0, $\Delta\omega$, and P_{diss} are the center frequency, offset frequency, and the power consumption, respectively. $L(\Delta\omega)$ is the phase noise at the specified offset frequency.

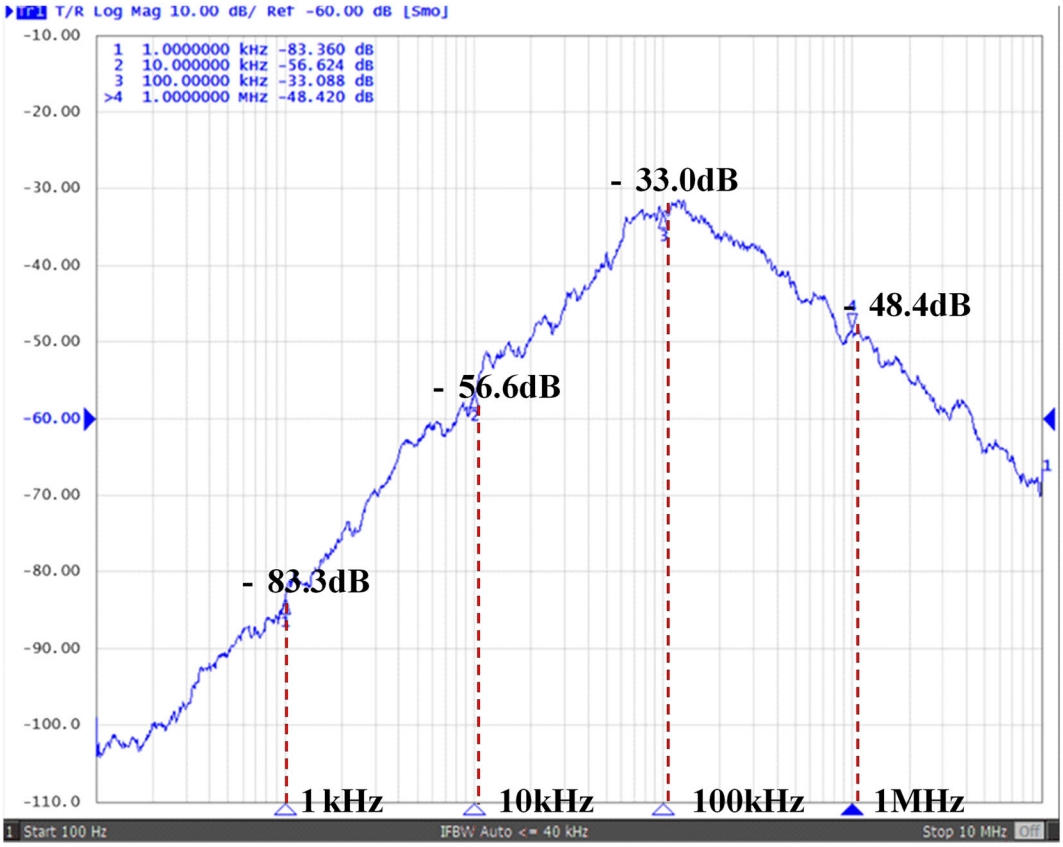

FIGURE 20 Measured PSRR of low noise low drop-out (LN_LDO) [Colour figure can be viewed at wileyonlinelibrary.com]

TABLE 2 Performance summary of frequency synthesizer

Ref	Pellerano et al[8]	Chiu, Chan, et al[9]	Chiu, Huang, et al[10]	This work
Process	250 nm CMOS	180 nm CMOS	180 nm CMOS	65 nm CMOS
Supply, V	2.5	1.8	1.8	1
FTR (%) (fosc) (GHz)	9.8% (5.4)	3.27% (5.5)	6% (5.43)	15.4% (5.585)
PN @ 1 MHz from fosc (dBc/Hz)	−116	−110.8	−114.28	−117
Power, mW	13.5	16.2	19.8	24
FOM_{PLL}, dBc/Hz	−179.35	−173.51	−176	−178.14
Area, mm^2	N/A	1.38	1.61	1

5 | CONCLUSION

This paper presents a 5.6-GHz low-noise frequency synthesizer for 5G applications. Herein, we propose a novel method to meet a target low phase noise performance for tight 5G applications. The VCO, which is a core block of the frequency synthesizer, uses a switched bias linear transconductance voltage-controlled oscillator structure. The fractional-N frequency synthesizer is sensitive to both current mismatch and noise in charge pumps. It is proposed that the noise generated in the charge pump will be minimized by the LF_SW. A MASH 1-1-1 DSM is used in order to minimize the noise components in the out-of-band. The phase noise of the frequency synthesizer is improved by multiplying the reference clock. The VCO phase noise is greatly affected by the output noise of the VCO phase noise and delta-sigma modulator noise. Therefore, using the low-noise on-chip LDO minimizes the phase noise degradation. This chip is implemented in a 65-nm CMOS process, and the die area is 1.0 mm^2. The measured tuning range of the VCO is about 15.4%, and the measured phase noise of the frequency synthesizer is −117 dBc/Hz at a 1-MHz offset from the carrier frequency of 5.585 GHz. Finally, the frequency synthesizer has a power consumption of 24 mW from a supply voltage of 1 V.

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