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Multilevel Bipolar Electroforming-Free Resistive Switching Memory Based on Silicon Oxynitride

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Abstract: Resistive random-access memory (RRAM) devices are fabricated by utilizing silicon oxynitride (SiO_xN_y) thin film as a resistive switching layer. A SiO_xN_y layer is deposited on a p+-Si substrate and capped with a top electrode consisting of Au/Ni. The SiO_xN_y-based memory device demonstrates bipolar multilevel operation. It can switch interchangeably between all resistance states, including direct SET switching from a high-resistance state (HRS) to an intermediate-resistance state (IRS) or low-resistance state (LRS), direct RESET switching process from LRS to IRS or HRS, and SET/RESET switching from IRS to LRS or HRS by controlling the magnitude of the applied write voltage signal. The device also shows electroforming-free ternary nonvolatile resistive switching characteristics having $R_{HRS}/R_{IRS} > 10$, $R_{IRS}/R_{LRS} > 5$, $R_{HRS}/R_{LRS} > 10^3$, and retention over 1.8×10^4 s. The resistive switching mechanism in the devices is found to be combinatory processes of hopping conduction by charge trapping/detrapping in the bulk SiO_xN_y layer and filamentary switching mode at the interface between the SiO_xN_y and Ni layers.

Keywords: bipolar; electroforming free; filamentary mode; multilevel; resistive switching

1. Introduction

As complementary metal-oxide-semiconductor (CMOS) technology is reaching its size limit, the traditional flash memory used in the present electronics industry is facing physical and technological difficulty in retaining charges in the reduced dimension [1,2]. The resistive random-access memory (RRAM) device, which has a metal-insulator-metal (MIM) structure, has shown huge potential as an alternative to the current nonvolatile memory due to its advantages of superior switching speed, low-power consumption, excellent reliability, and ultimate scaling potential with crossbar array architectures [3]. There has been extensive research on developing technologies to increase the storage density of RRAM, including physical scaling, a multiple stacked structure [4], and multilevel memory cells [5,6].

Among them, research on multilevel storage in a single memory cell has been actively conducted over the past few years. Multilevel storage behavior is particularly beneficial for high-density storage and oxide-based electronic synaptic devices [7,8]. Multilevel charge storage can be achieved by controlling the write voltage [9–11] or the write current [12].

Many combinations of MIM devices have demonstrated resistive switching properties. Among them, silicon-related dielectric materials have shown exceptional resistive switching properties [13,14] as well as compatibility with Si-based CMOS technology. SiO_xN_y appears to be a potential candidate for resistive switching memory devices due to the controllability of the band structure by controlling the composition of SiO_xN_y [15]. Kapoor et al. reported that the presence of oxygen in the silicon nitride layer increases the electron trap density in the metal/Si_xN_y/SiO_2/Si device [16], which makes SiO_xN_y a

more desirable candidate for resistive switching memory devices. Chen et al. explored the influence of oxygen on the performance of SiO_xN_y-based RRAMs and reported bistable resistive switching with a resistance switching ratio of about three after 100 cycles [17]. The effect of copper diffusion on the performance of SiO_xN_y-based RRAMs was investigated by Yang et al., who observed that the devices exhibit bistable resistive switching with an on/off current ratio of about $10^{1.5}$ with the aid of diffused copper after a two-step electroforming process. Without the copper layer, devices do not show any switching properties [18].

The most common bipolar resistive switching mechanism is the formation and rupturing of conductive filaments derived by voltage-driven ion migration [19]. Usually, an electroforming process is required to create the initial conductive filaments in a fresh device before repeatable resistive switching [20]. The electroforming voltage is much higher than the switching voltage after the electroforming process. The high electroforming voltage may induce severe mechanical and electrical stresses in the device, which changes the morphology of the films and possibly damages electrodes of the device [21]. It has also been observed that unexpected resistance states are generated due to the electroforming process, which degrades the device performance [22,23].

Evidently, electroforming-free operation is one of most desirable properties of the RRAM device for practical applications. There are two distinct characteristics of electroforming-free resistive switching. First, the resistances of the pristine state and high-resistance state (HRS) after the RESET process are similar. Second, the initial SET voltage and the succeeding SET voltage should be comparable. These characteristics are mostly credited to internal defects and conduction filament confinement [24]. The electroforming-free behavior has also been found by other researchers in nonstoichiometric metal oxides due to the presence of defects and oxygen ion migration [25,26]. To meet the abovementioned characteristics that require comprehensive defect profile control, ion doping [24], thermal treatment [27], optimization of the film thickness [28] and modulation of the fabrication process [24,29] have been investigated.

In this work, we studied electroforming-free operation as well as multilevel operation of a SiO_xN_y-based RRAM device. Defect-rich SiO_xN_y is employed as the resistive switching layer that is sandwiched between a p^+ silicon substrate and an Au/Ni metal layer. With the combination of the Ni layer and the defect-rich SiO_xN_y layer, we successfully incorporate an intermediate resistance state (IRS) between the HRS and low-resistance state (LRS) and eliminate the electroforming process, which requires a high activation voltage [18]. The device exhibits bipolar electroforming-free SET/RESET operational characteristics as well as multilevel digital memory characteristics with an HRS/LRS resistance ratio over 10^3, which is better than that of the SiO_xN_y-based devices introduced in previous reports [17,18].

In addition, the effect of current and silicon oxynitride thickness on the overall device performance is investigated. Finally, a feasible resistive switching model is proposed to describe the conduction mechanism of the device.

2. Materials and Methods

SiO_xN_y thin films with thicknesses of 7, 10, and 15 nm were deposited by plasma-enhanced chemical vapor deposition (PECVD)(Oxford plasmalab system 100 PECVD, Oxford Instruments Plasma Technology, UK, Plasma Technology, 66.7 mi · Yatton, Bristol, UK, BS49 4AP) on a p^+-Si substrate (boron-doped, 3.0 mΩ·cm) at 300 °C. The gas mixture, $N_2O/SiH_4/NH_3/N_2$ (60/400/20/600 SCCM), was supplied under a working pressure of 650 mTorr and an RF power of 15 W (30.6 W/mm^2). The heavily doped p^+-Si substrate served as the bottom electrode, and a circular-shaped Au/Ni (150/40 nm) top electrode with a radius of 50 μm was then deposited by e-beam evaporation through a shadow mask. To observe the area dependency, four different sizes of the 10-nm-thick SiO_xN_y-based devices were also fabricated with a radius of 35, 50, 150, and 225 um, respectively. Separately, 10-nm-thick SiO_xN_y films with the same composition were grown on a glass substrate for Fourier transform infrared (FTIR) absorbance spectroscopy measurement. The electrical characteristics

of the memory devices were measured using a semiconductor parameter analyzer (HP-4155A). (Hewlett-Packard Company, 3000 Hanover Street Palo Alto, CA 94304-1185 USA) Voltage was applied directly to the top electrode while the bottom electrode was grounded.

3. Results and Discussion

3.1. FTIR Measurement of the SiO_xN_y Film

The composition of the PECVD-deposited silicon oxynitride films depends on four major factors, (1) the N_2O gas flow rate, (2) the presence of N_2 gas, (3) the ratio of NH_3 in the gas mixture, and (4) the deposition temperature. As the literature suggests, the H–Si bond is weaker than the Si–O bond. The bond dissociation energies for H–Si and Si–O are 298.49 and 798 kJ/mol, respectively. Consequently, when the flow rate of N_2O and N_2 in the gas mixture is increased, oxygen replaces the hydrogen bound with silicon, and subsequently dominates in the film [30,31]. The resulting characteristics of the silicon oxynitride films appear to be more similar to oxide layers than nitride films [32].

It has also been reported that with a low flow rate of NH_3 and high deposition temperature (>200 °C), less hydrogen is incorporated into the deposited layer, and the electrical properties of the films are improved [33,34].

The results of the Fourier transform infrared (FTIR) absorbance spectroscopy of the SiO_xN_y film are shown in Figure 1. The most significant peaks at 850 and 820 cm^{-1} are assigned to the Si–N bond in silicon nitride, but is probably a combination of Si–N and Si–O–Si bonding in oxynitride [30,31]. The broadening of the Si–H absorption peak (2200–2300 cm^{-1}) is a result of the distortion of the S–H bonds, caused by the accommodation of both oxygen and hydrogen in the silicon oxynitride film [30]. The characteristic peak of N–H bonds (3300–3400 cm^{-1}) is absent, which indicates that hydrogen is only present in a small amount [32]. The FTIR spectra analysis confirmed that the characteristics of the SiO_xN_y film were dominated by oxygen and nitrogen, with little hydrogen [34].

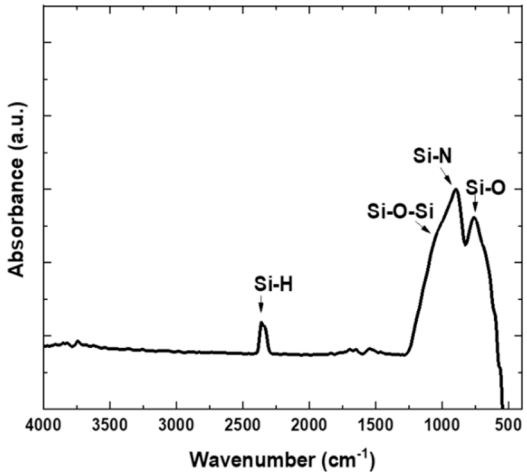

Figure 1. Fourier transform infrared (FTIR) absorbance spectra of silicon oxynitride film.

3.2. Electrical Characteristics

The I-V characteristics of the fabricated Au/Ni/SiO_xN_y/p^+-Si device were obtained by cycling the applied DC bias voltage according to the sequence of 0 V →+7 V →0 V →−7 V→0 V with a voltage step of 50 mV. The compliance current (I_{COMP}) was set to 0.25 mA for positive voltage bias. The multilevel switching operation of the 10-nm-thick SiO_xN_y based device (blue) is shown in Figure 2.

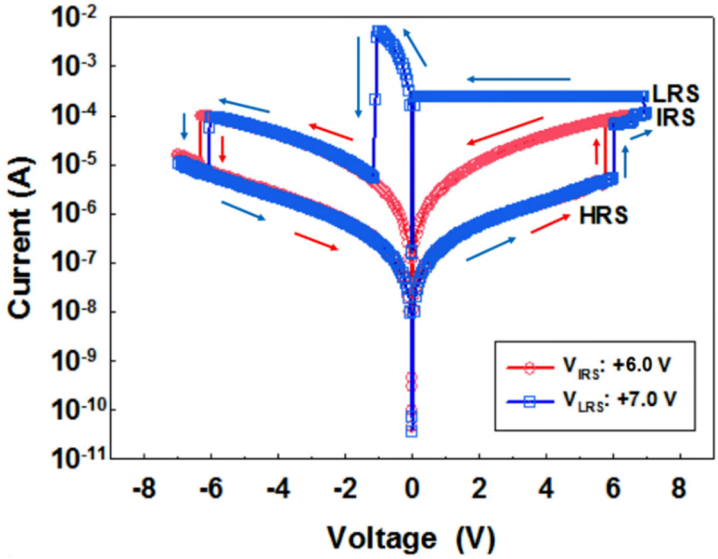

Figure 2. Typical I-V characteristics of an Au/Ni/SiO_xN_y/p^+-Si memory device with I_{COMP} = 0.25 mA.

The stability of the IRS was confirmed by cycling 0 V →+6.5 V →0 V →−7 V→0 V, which is shown in red. The I-V characteristics exhibit a pronounced electric hysteresis, which is a signature of resistive switching. In particular, it was observed that bipolar multilevel resistive switching can be obtained by controlling the magnitude of the applied voltage.

In the positive bias voltage region, the device was switched from the initial HRS to IRS at around +6 V, which is called V_{IRS}. As the higher positive bias voltage was applied to the device in the IRS, it leads to a sudden increase of current to the compliance current limit at around +7 V which is the LRS. In the negative bias voltage region, the current decreases abruptly when the applied voltage reaches around −1 V, leading to the first RESET process from the LRS to the IRS. As the negative bias voltage reaches −6 V, the second RESET process occurs from the IRS to the HRS.

The first SET and last RESET voltages of the full cycle of the I-V curve was almost the same as those of the intermediate cycle of the I-V curve. Additionally, the resistance of the initial state and HRS after the second RESET process are also the same (~10^7 Ω), which demonstrates the electroforming-free operational characteristics [24]. Detailed analysis and reasoning on the resistive switching, asymmetric behavior and electroforming-free behavior are discussed in the next subsection.

3.3. Resistive Switching Mechanism

A log(I)−log(V) plot of the 10-nm-thick SiO_xN_y-based device and current conduction process in the HRS, IRS, and LRS are shown in Figure 3.

The log(I)−log(V) characteristics of the device in the HRS and IRS can be clearly divided into different regions which are marked as R-1, R-2, and R-3. It follows the trap-controlled space charge-limited conduction (SCLC) mechanism [35,36]. On the other hand, in the LRS, which is marked as R-4, the log(I)−log(V) characteristics show an ohmic behavior with a slope of one, which follows the filamentary conduction. The characterization reveals that the resistive switching from the IRS to LRS is caused by controllable transformation from charge trapping/detrapping to filamentary conduction in the SiO_xN_y-based RRAM device.

The area-dependent current characteristics of Au/Ni/SiO_xN_y/p^+-Si memory devices is shown in Figure 4. The current of LRS does not depend on the area, which implies that the current conduction in LRS is dominated by the filamentary conduction. It also shows that the resistance switching mechanism between LRS and IRS is the formation and rupture of filaments. On the other hand, area-dependent I_{HRS} and I_{IRS} support that the current conduction in HRS and IRS is dominated by a trap-to-trap hopping process. [37,38].

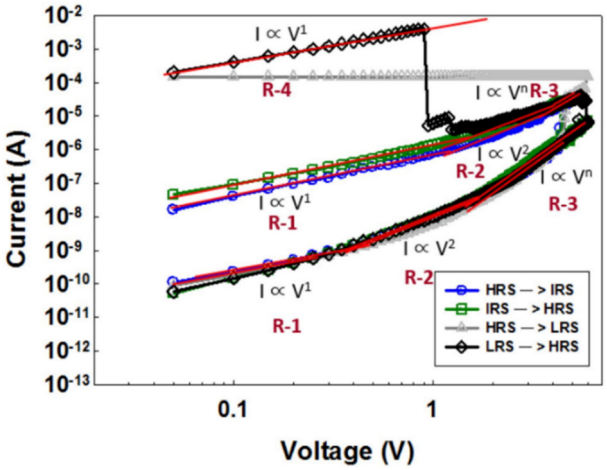

Figure 3. log (I) − log (V) characteristics of an Au/Ni/SiO_xN_y/p^+-Si memory device with I_{COMP} = 0.25 mA.

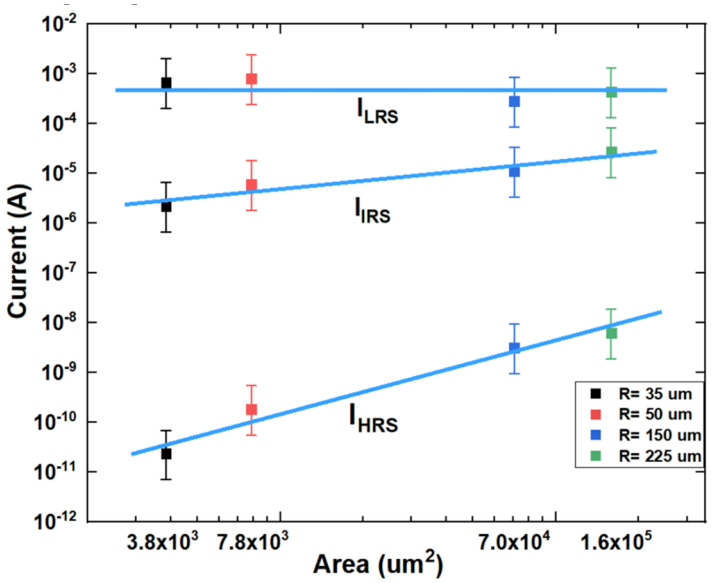

Figure 4. The area dependent current characteristics of Au/Ni/SiO_xN_y/p^+-Si memory devices.

Based on analysis of the current conduction mechanism by log (I) − log (V) plot and fitting, the total resistive switching mechanism of the device is proposed below, and the schematics are shown in Figure 5. For a detailed understanding of the switching mechanism, the switching from the HRS to IRS was named SET1 and IRS to LRS was named SET2. Similarly, the switching from the LRS to IRS was named RESET1 and IRS to HRS was named RESET2. The as-prepared Au/Ni/SiO_xN_y/p^+-Si memory device contained a certain number of defects in its active SiO_xN_y layer (Figure 5a). As positive bias voltage is applied, the SCLC is controlled by defects. The representative log(I)–log(V) characteristics of the SCLC usually involves two different regions. Ohmic conduction ($I \propto V$) is found in the low-voltage region (R-1). As soon as the voltage goes beyond the trap–filled limit (R-2 region), the log(I) − log(V) plot follows Child's square law ($I \propto V^2$). For further increase in voltage (R-3 region), the Pool–Frenkel emission helps the trapped electrons go to the conduction band by field-enhanced thermal excitation.

As the positive voltage reaches the SET1 voltage (V_{SET1}), the switching from the HRS to IRS takes place. The conduction path originates from the charge-trapping process of the electronic carriers through nitride-related traps in the bulk of the SiO_xN_y layer from the bottom electrode to the top electrode (Figure 5b) [35]. The traps are deep enough to store the trapped carriers for a sufficiently long time under repeated read operations. The potential barriers of the traps in the bandgap of the

switching oxide must be asymmetric with respect to the bias polarity or different levels of discrete trap states. As a result, the trapped carriers respond differently to the applied bias.

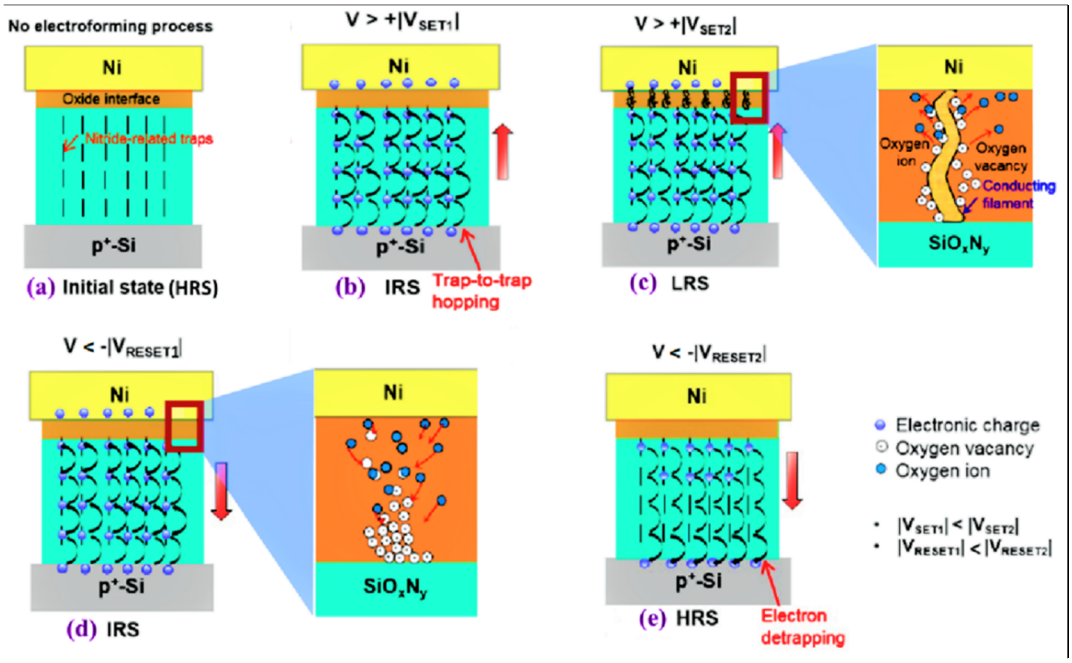

Figure 5. Schematics of the proposed switching mechanism of an Au/Ni/SiO_xN_y/p^+-Si memory device.

The electroforming-free resistive switching can be ascribed to the abundant initial nitride-related defects in the PECVD-deposited SiO_xN_y layer [17,30]. The defects, which are a combination of silicon dangling bonds, are considered as traps in the bulk of the initial SiO_xN_y layer [39]. The combination of oxygen and hydrogen with silicon dangling bonds results in a reduction of dangling bonds and traps [34,36]. Silicon dangling bonds and oxygen vacancies appear to play major roles for electroforming-free resistive switching.

A gas mixture of N_2O:SiH_4:NH_3:N_2 at a ratio of 3:20:1:30 and a nitrous oxide (N_2O) flow rate of 60 SCCM were applied during the PECVD deposition process, which resulted in an oxygen and nitrogen defect-rich SiO_xN_y layer with a low amount of hydrogen. This improved the electrical performance of the SiO_xN_y layer to the degree that it did not need any additional treatment to achieve electroforming-free resistive switching behavior in the device [34,36].

The switching mechanism is inherently related to the oxygen and nitrogen content in the film. When a positive voltage is increased beyond the V_{SET1} value and reaches the V_{SET2}, resistive switching from IRS to LRS takes place, and conductive filaments of oxygen vacancies (V_0^{+2}) are formed in the interfacial region between the Ni and SiO_xN_y layers. The Ni layer acts as a charge reservoir, because of its two stable (Ni^{2+}/Ni^{4+}) oxidation states [40,41].

Oxygen ions travel from the bulk SiO_xN_y layer to the Ni layer under the influence of the applied positive voltage to form nonstoichiometric NiO_x. Depending on their availability, oxygen ions can bond with Ni to form NiO, a Ni(O_2) complex, and/or nickel dioxide (ONiO) [42]. During the formation of NiO and NiO_2 the changes in the standard molar Gibbs free energy are −211.7 and −199.0 kJ mol^{-1}, respectively, at 289 K and 1 atmospheric pressure [43]. In electrochemical voltage units, the equivalents of these formation energies are 2.19 and 2.06 V, respectively [44]. The negative Gibbs free energies indicate that the formation of NiO_x is spontaneous.

The high oxygen vacancy density in SiO_xN_y can be attributed to Ni oxidation, which accumulates oxygen. Oxygen migration to the Ni layer causes a redox reaction within the conducting filaments, which stimulates the formation of more conductive oxygen vacancy filaments. It is possible that the formation of these conducting filaments occurs within or near the interface layer [45,46]. In any case,

the resistance of the device switches from the IRS to LRS when conducting filaments form in the oxygen-terminated interfacial region (Figure 5c).

To break the NiO_x bonds, the same amount of formation energy must be applied in the negative bias direction. The dissociation electrochemical voltages for NiO and NiO_2 are −2.19 and −2.06 V, respectively [43]. When a negative bias voltage is applied and approaches those values, the oxygen ions travel back from the Ni layer to the interface and recombine with the oxygen vacancies. This capture process ruptures the conducting oxygen vacancy filaments [47–49], leading to resistive switching from the LRS to IRS (Figure 5d). Therefore, no additional electroforming process is required to break the ultrathin NiO_x layer which is formed in the interfacial region between the Ni and SiO_xN_y layers. Regular bias voltage is enough to form and break the conduction filament through the ultrathin NiO_x layer. A similar phenomenon was reported by Tran et al., where the oxygen vacancy-based filament formation and annihilation were caused by the migration of oxygen ions/vacancies at the interfacial layer between the Ni electrode and the active oxide layer depending on the bias voltage [50].

The I-V characteristics in Figure 2 are asymmetric because the voltages required to form and rupture the conducting filaments are different. The SET2 process needed to form a complete conducting filament requires more energy than the RESET1 process. In RESET1, the conducting filament of oxygen vacancies is partially ruptured at the weakest point of the filament, changing the resistance state from LRS to IRS [11,12].

A further increase in the negative bias voltage leads to the RESET2 voltage (V_{reset2}), where detrapping of the electronic carriers becomes prominent. Here, the conduction path is broken by a charge-detrapping process, and by electronic carriers hopping back through the nitride-related traps of the SiO_xN_y layer from the top to the bottom. In turn, the resistance state of the device switches from the IRS to HRS (Figure 5e) [35].

The magnitudes of the voltages required for the SET1 and RESET2 processes are essentially the same because in both cases charges have to cross almost the same distance by hopping [35].

3.4. Effect of Write-Current Level and Silicon Oxynitride Thickness

The amount of current that passes through the device needs to be controlled to avoid permanent breakdown during the switching process of the device. It has also been reported that the size and number of conductive filaments can be controlled by the write current in filamentary switching mode [51,52].

The influence of the write current on the resistive switching characteristics of the Au/Ni/SiO_xN_y (10 nm)/p^+-Si device is shown in Figure 6, with four write current limits of 0.1, 0.15, 0.25, and 100 mA.

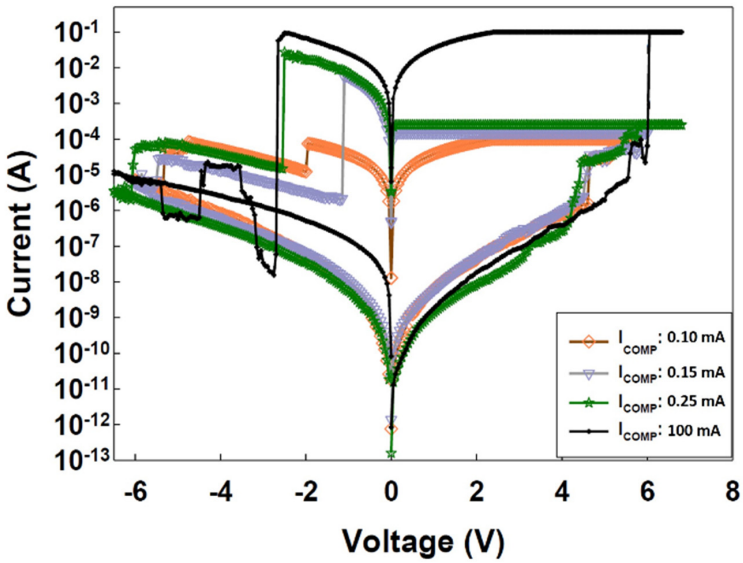

Figure 6. I-V characteristics of Au/Ni/SiO_xN_y/p^+-Si memory device with various I_{COMP} levels.

The device shows stable multilevel resistive switching states, and the two SET voltages and the second RESET voltage are almost the same regardless of the write currents of 0.1, 0.15, 0.25 mA. This can be attributed to the presence of enough defects in the SiO_xN_y.

As the write current increases, the LRS current of the device also increases at the same second SET voltage. This implies that multiple states can be programed by using different levels of write currents. Even at the same SET voltage, the resistance states can be altered by changing the write current level.

However, the device loses multilevel operational characteristics and shows only bistable resistive switching behavior when the device is subjected to the write current of 100 mA. The IRS state does not exist anymore. This indicates that the resistive switching mechanism may change completely from charge trapping and trap-to-trap hopping to filamentary switching inside the bulk SiO_xN_y after the device conducts current as high as 100 mA. The most apparent reason could be that the intrinsic defect sites involving charge hopping conduction in the IRS are damaged by the formation of large conductive filaments. The effects of write current on the resistance switching mechanisms were also observed by other researchers [53,54]. Based on these results, it is inferred that the resistive switching from the HRS to LRS is correlated with the filamentary model.

The I-V characteristics of SiO_xN_y-based memory devices having various SiO_xN_y thicknesses are compared in Figure 7. The device with a 15-nm-thick silicon oxynitride layer shows a higher HRS, IRS, and LRS current than the devices with thinner layers, which implies that the 15-nm-thick SiO_xN_y switching layer more likely hosts more nitride-related traps and oxygen vacancies. A similar phenomenon was reported in [35] and [55], where a thicker oxide layer and silicon nitride layer hosted more oxygen vacancies and more nitride-related traps, respectively. Therefore, the conductivity of the 15-nm-thick SiO_xN_y layer is higher than those of the thinner layers. As a result, the formation of conductive paths is easier in the 15-nm-thick SiO_xN_y layer than in a 10- or 7-nm-thick layer [56].

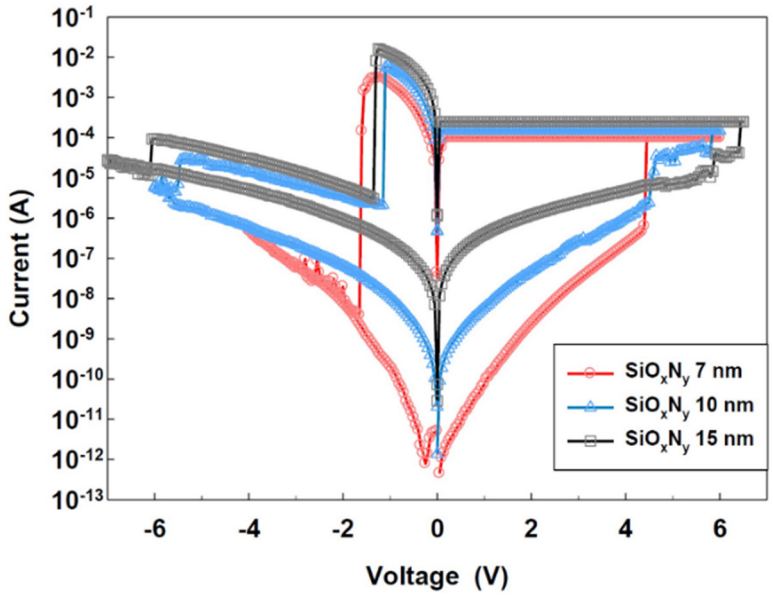

Figure 7. I-V characteristics of Au/Ni/SiO_xN_y/p^+-Si memory devices with various SiOxNy thicknesses.

The SET and RESET voltages for the IRS of the device increase with the increased SiO_xN_y layer thickness, which is attributed to the increased number of nitride-related traps and oxygen vacancies in the layer [35]. Meanwhile, the device with a 7-nm-thick silicon nitride layer does not show multilevel switching behavior but rather an electroforming-free bistable resistive switching behavior.

The thickness dependency of the multilevel resisting switching of the RRAM can be explained with the proposed model presented in Figure 5. According to the resistive switching model, the conduction mechanism for the HRS to IRS is due to the trap-to-trap hopping process of the charge carriers and the IRS to LRS is the filament formation at the interface of the Ni and SiO_xN_y layers. A certain thickness of

the SiO_xN_y layer is required for the charge carriers to travel by hopping trap-to-trap from the bottom electrode to the interface of the Ni and SiO_xN_y layers. If the thickness of the SiO_xN_y layer is less than the required thickness, the charge carriers can easily move to the interface by tunneling with the small amount of positive bias voltage. Furthermore, the filament formation mechanism takes place which causes the device changing from the HRS to LRS, eliminating the IRS state. As a result, the IRS state is not observed in the 7-nm-thick SiO_xN_y-based device. It shows a direct change from the HRS to LRS at lower bias voltage than that of the 10-nm-thick SiO_xN_y-based device.

The thickness-dependent resistance switching analysis shows that a certain thickness (10 nm) of the SiO_xN_y layer is essential to form the IRS state as well as to obtain three resistance states when the device is fabricated using the process mentioned in this study because the amount of traps and oxygen in the SiO_xN_y depends on its thickness. The thickness-dependent resistive switching was also reported by other researchers [57,58].

3.5. Endurance and Retention Characteristics

The DC endurance of the Au/Ni/SiO_xN_y (10 nm)/p^+-Si memory device is shown in Figure 8. The devices were measured under a compliance current of 0.15 mA and a read voltage of −0.5 V.

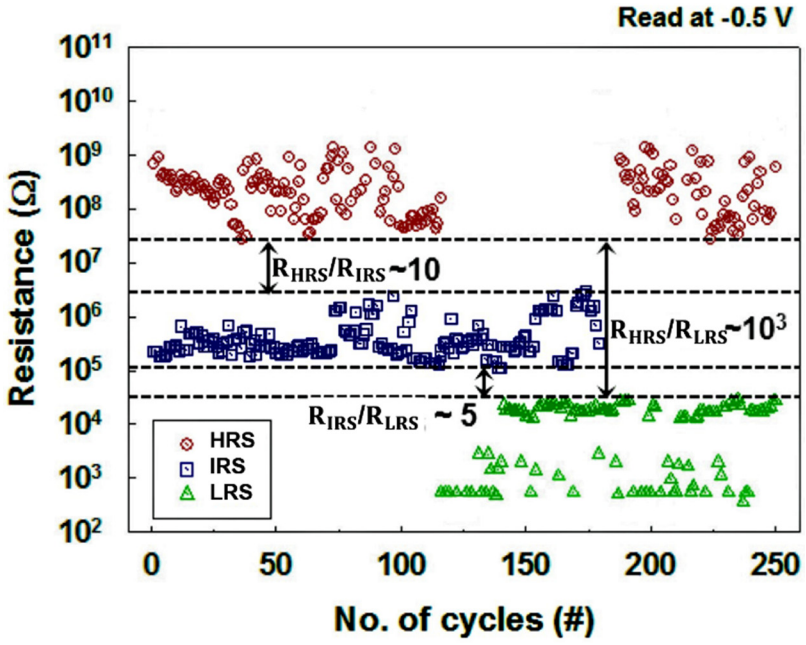

Figure 8. DC endurance property of the Au/Ni/SiO_xN_y/p^+-Si memory device.

Under a positive voltage bias, the LRS state is controlled by the compliance current. To obtain the actual LRS current value, a negative bias voltage region was chosen to read values, as there is no compliance current during negative bias. The voltage for RESET1 can vary by −2 to –1 V, depending on differences in thickness and compliance current. Consequently, −0.5 V was selected as the read voltage, to ensure that the measured current was not affected by the compliance current.

To assess the memory device, a total of 250 DC cyclic measurements were performed successively. To confirm the stability of each state, the first 120 cycles were performed while switching between HRS/ IRS, the next 60 cycles were performed between IRS/ LRS, and the last 70 switching cycles were performed between HRS/ LRS. The measured resistance ratios of the various states, R_{IRS}/R_{HRS}, R_{LRS}/R_{IRS}, and R_{IRS}/R_{HRS}, were found to be larger than 10, 5, and 10^3, respectively.

In addition, to check the pulse endurance property of the memory device, the SET voltage pulse (+6.0 V, 100 ms) and RESET voltage pulse (−6.8 V, 100 ms) were generated by a waveform generator, and the device state was monitored by using the read pulse (−0.5 V, 100 ms). The pulse endurance of up to 50 cycles for switching between the HRS and IRS was obtained on the SiO_xN_y device as shown

in Figure 9. The results show quite distinct HRS and IRS state currents as well as device operation at a low current level.

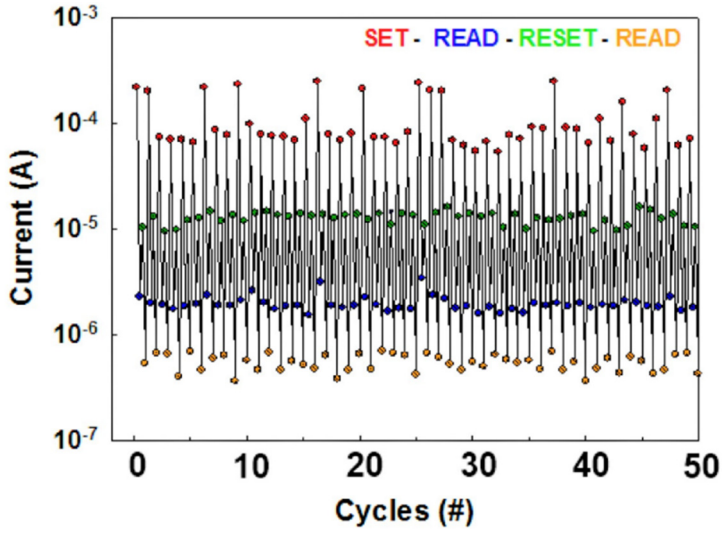

Figure 9. Pulse endurance property of the Au/Ni/SiO_xN_y/p^+-Si memory device.

The typical retention behavior of the device is shown in Figure 10 under a reading voltage of −0.5 V. The device shows excellent retention characteristics as the resistance values in the HRS, IRS, and LRS show no degradation over 1.8×10^4 sec at 120 °C.

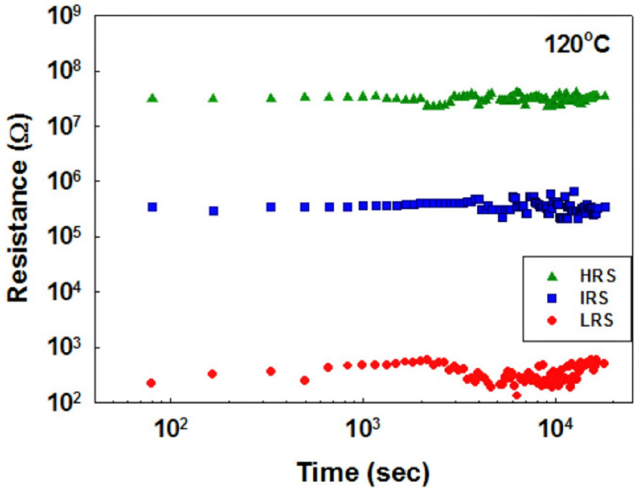

Figure 10. Retention property of the Au/Ni/SiO_xN_y/p^+-Si memory device.

4. Conclusions

A silicon oxynitride (SiO_xN_y)-based nonvolatile resistive switching memory device exhibiting electroforming-free, multilevel bipolar switching characteristics was successfully fabricated by employing a p^+-Si substrate and Au/Ni as the bottom and top electrodes, respectively. The device exhibits multilevel resistive switching from HRS to IRS, IRS to LRS, HRS to LRS, and vice versa. The switching mechanism was explained based on the I-V characteristics of the devices. The resistive switching between HRS and IRS is attributed to the electronic charge trapping and detrapping from the defects present in the bulk SiO_xN_y layer. The resistive switching between the IRS and LRS is attributed to the formation and rupture of filaments at the Ni/SiO_xN_y interface region. Both types of switching can be controlled by the magnitude of the applied voltage and the compliance current. The variation of the write current influences the switching performance in the filamentary mode of the interface region, and the variation of the thickness affects the switching performance in the bulk SiO_xN_y layer.

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