Foreword Special Issue on "New Simulation Methodologies for Next-Generation TCAD Tools"

TECHNOLOGY computer-aided design (TCAD) is an integral part of the development process of semiconductor technologies and devices, a field which has become increasingly complex and heterogeneous. Processing of integrated circuits requires nowadays over 400 process steps, and the resulting devices often have an intricate 3-D structure and contain various specifically designed materials. The full device behavior can only be understood by considering effects on all length scales from atomistic (material properties, interfaces, defects, and so on), to nanometric (quantum confinement, non-bulk properties, tunneling, ballistic transport, and so on), to full-chip dimensions (strain, heat transport, and so on), and time scales from femtoseconds (scattering, ferroelectric switching time, and so on) to seconds (trapping times, degradation, and so on). Voltages, currents, and charges have been scaled to such low levels that statistical effects and process variations have a strong impact. Devices based on new materials (e.g., 2-D crystals) and physical principles (ferroelectrics, magnetic materials, qubits, and so on) challenge standard TCAD approaches. While the simulation methods developed by the physics community can describe the basic device behavior, they often lack important simulation capabilities like, for example, transient simulations or integration with other TCAD tools, and are often too slow for daily use. Due to the complexity of semiconductor technology, it becomes more and more difficult to assess the impact of a change in processing or device structure on circuit performance by looking at a single aspect of an isolated device under idealized conditions. Instead, a TCAD tool chain is required which can handle realistic device structures embedded in a chip environment. New methodologies are required for all aspects of TCAD to ensure an efficient tool chain covering from atomistic effects to circuit behavior based on flexible simulation models that can handle new materials, device principles, and the ensuing large-scale simulations and that make use of artificial intelligence for well-chosen (sub)routines to decrease the overall simulation time. This Special Issue features six invited and 18 regular papers that address these problems.

In the first invited paper, M. Stettler *et al.* review the application of the TCAD tool chain to process and device development. The tool hierarchy starts at the atomistic level with quantum mechanical simulations for material design and ends at the chip level for which, for example, the operating temperature is calculated to estimate device degradation. It is shown how the simulation programs of the different levels are linked to obtain short turn-around times as well as reliable results.

E. M. Bazizi *et al.* discuss in their invited paper the development of a material-to-system co-optimization platform aimed at maximizing the chip performance, and at minimizing the occupied area and power consumption at the same time. At the system level, even the impact of algorithms, software, and applications can be considered to select the best technology and devices.

In the third invited paper by C. Jeong *et al.*, the application of machine learning to the TCAD tool chain is discussed, and it is shown that the combination of artificial intelligence and TCAD enables large-scale and high-throughput simulations not possible before. For example, tunneling can be described by a simpler but more CPU-efficient and robust model based on machine learning, where a part of the physics-based model is replaced by a neural network.

A. Afzalian *et al.* describe in the fourth invited paper the development of an advanced DFT-NEGF simulator for MOSFETs based on 2-D materials in which the error-prone step of matching simpler Hamiltonians to the *ab initio* methods is avoided. With this fundamental tool, standing at the basis of the TCAD tool chain, they explore novel materials and device concepts.

In the fifth invited paper by G. Eneman *et al.*, TCAD is utilized to investigate the dependence of the mechanical stress in SiGe nanowires on the layout and quality of the epitaxial source/drain stressors based on simulations that are modeled according to the process flow developed by a major research institution.

In the sixth invited paper L. Codecasa *et al.* show how to exploit CPU-efficient algorithms to derive from a 3-D thermal simulation, which covers length scales differing by many orders of magnitude, the structure function of a high-speed SiGe HBT required for generating a thermal compact model that can be used to explore the impact of self-heating at the circuit level.

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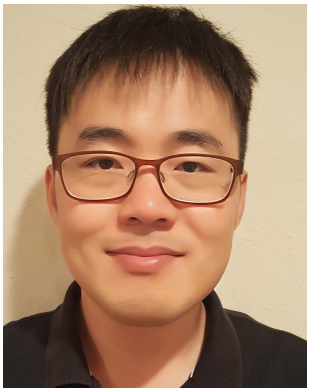

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