A three-stage capacitor-less low noise LDO regulator for DCO phase noise reduction

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A phase noise reduction technique is presented in a three-stage capacitor-less (CL) low dropout (LDO) regulator. This paper proposes a simple RC network that reduces the noise from both bias generation and inside the LDO. This LDO is applied to a conventional CMOS LC oscillator and achieved 3 dB reduction of phase noise at 1 MHz offset from 20 GHz output. The line and load regulations are, 90 μV/V and 0.013 μV/mA, and the output noise at 1 MHz is 6.6 nV/$\sqrt{\text{Hz}}$.

Introduction: Oscillators are essential for wireless and wired communication and the phase noise of oscillators should be low enough to guarantee secure and reliable data communication [1]. However, the phase noise of the oscillator is greatly sensitive to supply noise. Therefore, it is important to design a low noise low dropout (LDO) with high line regulation and load regulation. A conventional low noise LDO makes a narrow bandwidth (BW) to filter out the LDO noise by using a one-stage error amplifier (EA) with an RC filter that ensures the loop stability at the cost of small DC gain that results in poor load and line regulation. Furthermore, they require large on-chip capacitors (140 and 250 pF) that lead to a low BW for noise and ripple reduction [2]. For on-chip integration, the LDOs with small capacitors are preferred and a capacitor-less (CL) LDOs is reported by placing a dominant pole inside the LDO, which relaxes the size requirement of the load capacitor [3]. Additionally, to enhance the load regulation and line regulation, a multi-stage amplifier with a large gain LDO structure is required with compensation techniques for stability. For example, a CL LDO with a three-stage topology utilizes a nested Miller compensation and damping-factor-control frequency compensation (DFC) for wide BW, but poor output noise is observed in CL LDO configuration, of which the noise is not sufficiently low for oscillator supply [4]. This paper proposes a noise reduction technique with a simple RC network that is applied to a three-stage LDO and improves oscillator phase noise by more than 3 dB.

LDO design: Figure 1 shows the schematic representation of the proposed LDO regulator in the 65 nm CMOS technology. The size of the N-type MOS (NMOS) pass transistor set to (10 mm/280 nm) allows the maximum load current of 100 mA. $R_{f1} = 100$ kΩ, R_{f2} is designed to support various output levels by controlling the feedback factor with a fine step. A four-bit control adjusting R_{f2} from 100 kΩ to open is implemented through serial peripheral interface (SPI) control.

The EA consists of three stages. By using three-stage EA, LDO can obtain a higher gain compared to two-stage EA, but it consumes more current. To reduce the g_m of the first stage of EA, V_B was set high. A small g_m and a large C_M of 30 pF make unity gain frequency (UGF) low because it is determined by g_m/C_M [5]. The low UGF allowed to reduce the output noise of the LDO. In the output noise contribution, the noise from *M8*, which is significant unlike the tail current source that would be

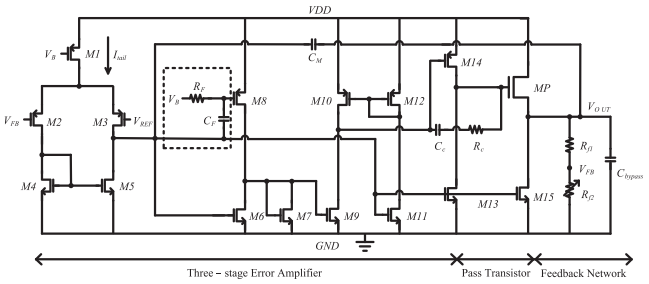

Fig. 1 *Schematic representation of the proposed LDO regulator*

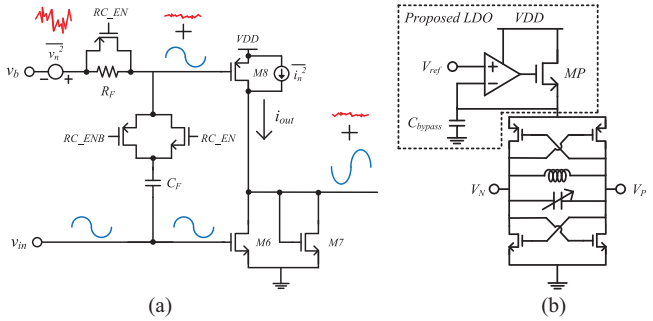

Fig. 2 *Noise reduction technique in (a) transconductance-boosting circuitry and (b) CMOS LC oscillator with the proposed LDO*

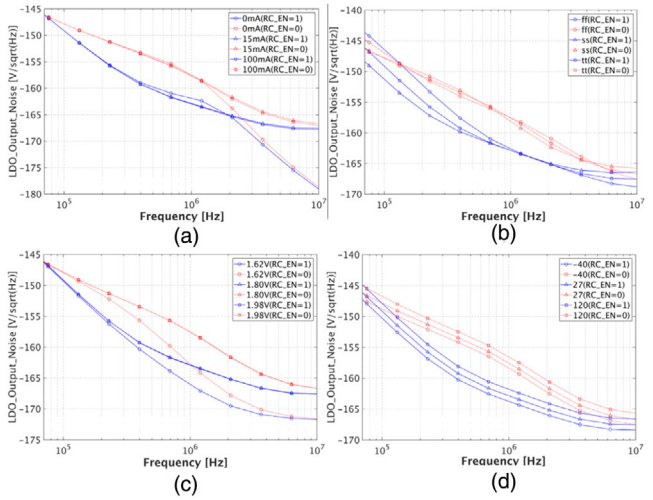

Fig. 3 *LDO output noise reduction by the proposed technique (a) load variation (0 mA, 15 mA, 100 mA), (b) process variation (ff, ss, ff), (c) supply variation (1.62 V, 1.8 V, 1.98 V), and (d) temperature variation (–40°C, 27°C,120°C)*

suppressed by the differential pair, is the dominant problem. This noise problem is significantly alleviated by the proposed RC network.

Proposed noise reduction technique design: Figure 2a shows the proposed RC network implemented to the gate of *M8* with $R_F = 500$ kΩ and $C_F = 9.6$ pF. This network reduces noise contribution from *M8* by loading the signal at frequencies above $1/(2\pi R_F C_F)$ without changing the bias current. The transfer function from v_{in} to *M8* drain current (i_{out}) is found by the following:

$$\frac{i_{\text{out}}}{v_{\text{in}}} = -g_{m8}\frac{sR_FC_F}{1+sR_FC_F}, \tag{1}$$

which is a high-pass filter in the signal path.

Additionally, the noise coming from v_b, generated by the bias circuit, is filtered out by the low pass filter. Because the gate node of *M6* becomes low impedance due to the large Miller capacitor (C_M), v_{in} is considered as an AC ground and the transfer function from v_b to i_{out} is found as shown in Equation (2),

$$\frac{i_{\text{out}}}{v_b} \approx -g_{m8}\frac{1}{1+sR_FC_F}, \tag{2}$$

which is a low-pass filter that suppresses the noise from the bias.

Figure 2b shows the schematic of the LC oscillator and the proposed LDO. The LDO with 22 pF load capacitor (C_{bypass}) is connected to the CMOS LC oscillator. VDD is 1.8 V, and the output voltage of LDO is 1 V and the R_{f2} is set to open to have a unity gain for low noise.

Figure 3 shows the output noise comparisons of the LDO by the RC network in various variations. The BW of the LDO is set to 30 kHz with $I_{\text{tail}} = 300$ nA, the output noise is seen lower significantly around the

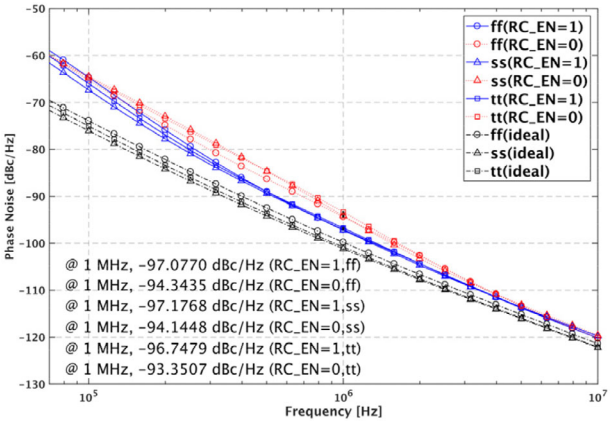

Fig. 4 *Phase noise reduction in 20 GHz DCO by the proposed technique*

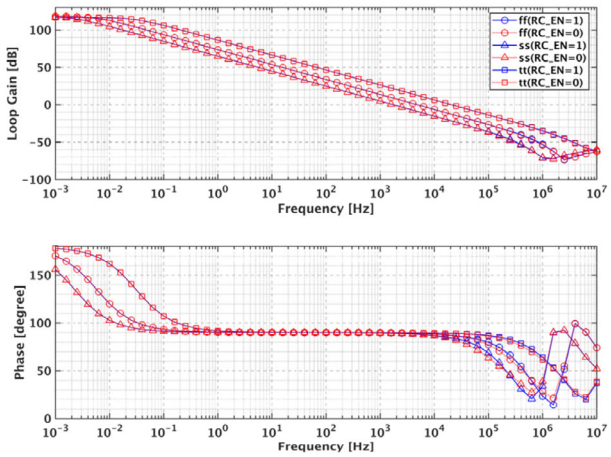

Fig. 5 *Open-loop AC response of LDO*

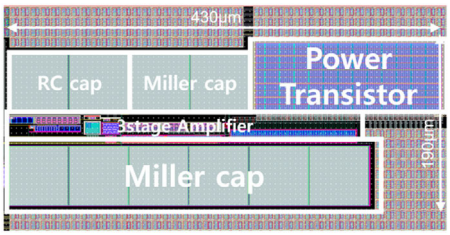

Fig. 6 *Layout*

pole frequency of 33 kHz formed by R_F and C_F. As shown in Figure 4, the phase noise of the LC oscillator is also improved by about 3 dB.

Figure 5 shows the AC response of the proposed LDO when VDD is 1.8 V, LDO output voltage is 1 V and load current is 15 mA. The LDO is stable in several corners. The pole frequency of the RC network is placed near UGF. The UGF is unaffected by the RC network, moreover, the phase response is slightly improved by the feedforward path by the RC network.

The active area is 430 μm × 190 μm as shown in Figure 6. The CL LDO even with the small load capacitor of 22 pF has achieved the low integrated output noise, comparable to that of LDO with a large off-chip capacitor [6]. Using the proposed RC network, the output noise at 1 MHz is reduced by 1/2 compared to the disabled RC network. Also, using three-stage EA, the load and line regulation are improved to 0.013 μV/mA and 90 μV/V respectively. When the load current is changed from 1 to 100 mA in 1 μs, the variation of LDO output voltage is 31 mV. The FOM in Table 1 is specified according to [8]. Table 2 summarises our noise performance variation due to device mismatch.

Conclusion: A noise reduction technique in a three-stage CL low noise LDO regulator is presented in this letter. A simple RC network reduces the noise within the amplifier by the increased g_m of the second stage and the noise outside the amplifier coming from the bias by low pass filtering.

Table 1. Comparison of CMOS LDO regulators

	[6] 2017[a]	[7] 2019[a]	This work[b]
Process (nm)	130	500	65
Input Voltage (V)	1.05∼2.0	1.5∼5	1.25∼3
Output Voltage (V)	1.0	1.3∼4.8	1∼1.6
Dropout (mV)	29.7	200	>250
C_{Load} (pF)	10^6(off-chip)	5.1(on-chip)	22(on-chip)
$I_{Load,max}$ (mA)	300	600	100
$I_{Quiescent}$ (μA)	14-120	>16.5	20-114
Load regulation (μV/mA)	6	11	0.013
Line regulation (μV/V)	440	156	90
Output noise (1 MHz) (nV/$\sqrt{\text{Hz}}$)	-	-	6.6
Integrated output Noise (10 to 100 kHz) (μV_{rms})	80	-	80
Active area (mm^2)	0.1825	0.082	0.0817
FOM[c] (fs)	12440	0.12	1.36

[a]Measurement result.
[b]Post layout simulation result.
[c]$FOM = (C_L \cdot \Delta V_{out} \cdot I_Q)/I^2_{L,max}$

Table 2. Monte Carlo noise results of the proposed technique

Output noise (1 MHz) (nV/$\sqrt{\text{Hz}}$)	RC_EN = 1		RC_EN = 0	
	Mean	Deviation	Mean	Deviation
	6.6	0.233	12.3	0.383
Integrated output Noise (10 to 100 kHz) (μV_{rms})	Mean	Deviation	Mean	Deviation
	83.48	0.882	82.81	0.946

The low noise CL LDO is utilized in supply noise sensitive circuits like LC oscillators and the significant phase noise improvement is achieved without scarifying load/line regulation performance by three-stage EA.

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