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RESEARCH ARTICLE

A 13-Bit 1-MS/s SAR ADC With Completion-Aware Background Capacitor Mismatch Calibration

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ABSTRACT This paper introduces a completion-aware background sequential capacitor mismatch calibration technique for SAR ADC. The proposed method sequentially corrects capacitor mismatch from the lower to the upper bits in the CDAC. This calibration method can automatically detect when calibration is complete, thereby improving power efficiency by terminating calibration activities. This approach mitigates the trade-off between adaptation speed and calibration code variation, enhancing correction speed. Moreover, the sequential calibration demonstrates stable adaptation in unpredictable input environments. The ADC developed in this study utilizes 55-nm ultra-low power (ULP) CMOS technology, operates at a speed of 1 MS/s, and consumes 43 μW of power. It achieves peak DNL of $+0.83/-0.62$ LSB and INL of $+1.89/-1.13$ LSB. Furthermore, it achieves a mean SNDR of 68.5 dB and SFDR of 83.8 dB, resulting in a FoM of 19.59 fJ/conv.-step.

INDEX TERMS Analog-to-digital converter (ADC), successive approximation register (SAR), capacitor mismatch, background calibration.

I. INTRODUCTION

The successive approximation register (SAR) ADC is widely used in various low-power, medium-to-high resolution applications, such as Internet of Things (IoT), mobile applications, bio-sensors, and touchscreen panel drivers [1], [2], [3]. Some applications require tens of ADCs for multiple channels, where a small area design is essential for a low-cost implementation. One of the key performance limitations of a typical SAR ADC is its linearity, which is influenced by the capacitor mismatch in a capacitive digital-to-analog converter (CDAC). A large CDAC area is required for better matching, degrading energy efficiency, and increasing settling time and system cost. Hence, the capacitor mismatch calibration is a promising solution to achieve a higher figure-of-merit (FoM) [4], [5], [6], [7], [8].

The mismatch calibration consists of mismatch detection and correction phases. There are two types of detection methods: background and foreground-based methods. Foreground calibration needs a start-up calibration time before the normal conversion and requires specific input conditions such as ideal clean reference or input shorting [9]. In contrast, background calibration does not interrupt the normal ADC operation during calibration. However, background calibration requires a longer settling time than foreground calibration and depends on input behavior. In the correction phase, analog [7] and digital [5], [6], [10] methods exist.

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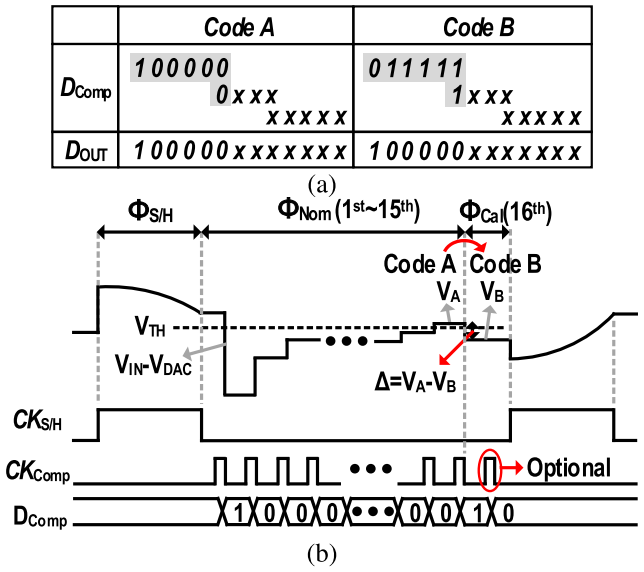

FIGURE 1. Illustration of (a) redundancy inside an ADC and (b) mismatch detection mechanism.

Foreground calibration provides consistent calibration behavior for known calibration signals but lacks time efficiency as it requires the ADC to pause during calibration. On the other hand, background calibration can operate without interfering with normal conversion operations. However, the calibration process might degrade performance if input characteristics are inconsistent. Especially in applications where multiple channels share input, differences in calibration time between channels can cause problems during digital processing.

This paper proposes a background sequential capacitor mismatch correction SAR ADC with a feature that can detect calibration completion. This method lets us know the instant at which calibration is completed through a calibration done detector. After calibration is completed, one cycle of comparison time (ϕ_{Cal}) in Fig. 1(b) can be assigned to the normal conversion cycle so that the additional conversion time is secured as a time margin in the case where the longer decision time is needed by comparator metastability or used as additional bit conversion. Additionally, the proposed calibration method shows faster convergence in response to input signal conditions than traditional background methods, making it suitable for various applications. Although foreground calibration has limitations in tracking voltage or temperature variations, the proposed method allows for intermittent recalibration after calibration completion using the calibration done signal, enabling the tracking of environmental changes.

This paper is organized as follows. Section II introduces the proposed mismatch calibration, and implementation details are described in Section III. Section IV describes the measurement result of the ADC, and section V concludes the paper.

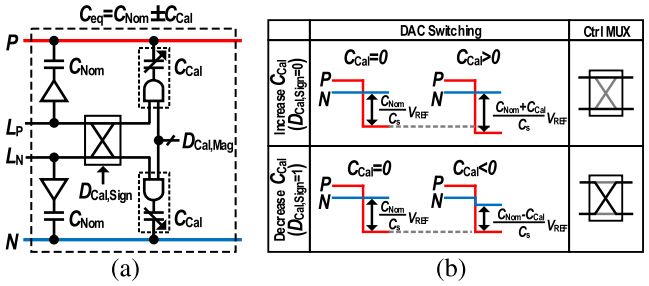

FIGURE 2. Illustration of (a) the mismatch correction driver and (b) operation of mismatch correction.

II. MISMATCH CALIBRATION

A. PREVIOUS ART

Capacitor mismatch calibration is crucial for enhancing linearity in small-area, low-power SAR ADCs [4], [5], [6], [7]. In this section, we will review several capacitor mismatch calibration methods.

In [6], a foreground calibration technique is presented. This fully digital method eliminates the need for an accurate reference or input signal. The method finds application in a sub-2 arbitrary-radix SAR ADC, which leverages integer weights to simplify the architecture. The calibration algorithm quantifies non-linear code jumps and outlines a procedure to rectify the MSB mismatch. However, foreground calibration needs to stop the ADC operation, and there are limitations to the calibration resolution. The capacitor swapping scheme in [11] effectively reduces the integral nonlinearity (INL) error in SAR ADC. The MSB capacitor mismatch for half of the input samples leads to an INL error for both negative and positive input samples. This error reverses for the remaining half of the input samples. The swapping between these two INL errors effectively lowers the average INL error. However, the complexity of the logic is high compared to the degree of performance improvement. The histogram-based calibration method in [12] utilizes histogram windowing to identify capacitor mismatch. This approach measures the average bin count within a window and adjusts the bit weight digitally. However, it requires uniformly distributed input and might take a significant time to calibrate due to the need to count the overall bin count. In [13], the mismatch error shaping (MES) technique for oversampling SAR ADCs combines elements of flash, SAR, and delta-sigma modulation, eliminating the need for factory trimming or digital calibration, although the overall architecture is complex. The digital calibration for split-CDAC SAR in [14] avoids the need for an analog calibration DAC by determining calibration error codes using another split-CDAC. Lastly, a time-interleaved (TI) ADC architecture in [15] incorporates a charge injection cell DAC and utilizes neural-network calibration to correct multiple sources of errors in TI-ADC.

The SAR ADC in [7] uses redundancy for mismatch calibration. To illustrate the MSB five-bit calibration, we assume that the normalized weight of the MSB seven-bit

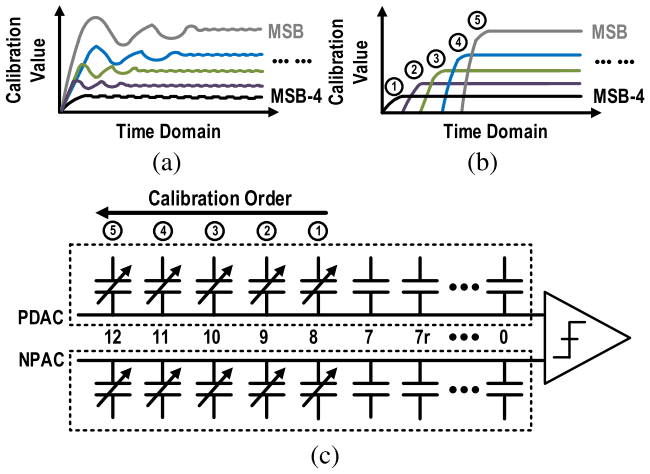

FIGURE 3. Coefficient settling diagram of (a) existing [7], (b) proposed sequential calibration, and (c) proposed correction sequence diagram.

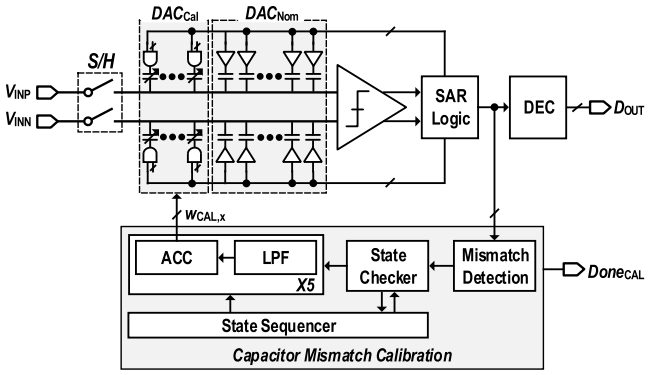

FIGURE 4. Block diagram of the proposed SAR ADC incorporating a mismatch calibration block.

is $W = \{32,16,8,4,2,1,1\}$, inclusive of the redundancy bit of the 7_{th} bit. Therefore, the two codes $B_1 = \{1,0,0, 0,0,0,0,x,\cdots,x\}$ and $B_2 = \{0,1,1,1,1,1,1,x,\cdots,x\}$ yield the same digital output, assuming linearity of the ADC in Fig. 1(a). Unlike conventional methods such as those described in [4], [5] and [6] that require comparison against an external reference voltage or internally generated zero input, our approach internally performs mismatch detection and correction based on specific codes in Table 1 to correct the specific MSB capacitor mismatch errors. When mismatch detection codes are encountered, they trigger the relevant bit's calibration cycle (16_{th}). CDAC driver data switch between two codes in Table 1 and monitor the comparator output to find the mismatch direction [7]. However, this approach needs a long convergence time and code fluctuation due to the simultaneous calibration of multiple bits and an inability to determine calibration completion.

B. PROPOSED CALIBRATION

Among various background mismatch calibration methods, using CDAC with redundant conversion is effective for mismatch detection [7]. The calibration process in the ADC explicitly targets the upper five MSB bits due to their significant effect on performance and substantial mismatch errors. The calibration method detects differential nonlinearity (DNL) errors representing capacitor mismatch by utilizing inherent redundancy. If there is no mismatch, the sum of the activated codes A and B, denoted by V_A and V_B, will be the same, as illustrated in Table 1. Conversely, if a mismatch error exists, the DAC voltage between the two codes will differ. As illustrated in Fig. 1(b), after 15 cycles of normal conversion, the process compares the conversion code of the upper seven MSBs with mismatch activation patterns in Table 1. Code A and Code B are numerically identical due to redundancy. If the top seven bits match code A, the internal DAC switches to code B, and an additional conversion is conducted in the 16th cycle to detect a mismatch. If code B is detected, the internal code changes to code A. When the capacitors are ideal, the results of the last cycle (D_{15}) and the additional cycle (D_{16}) should match. Any mismatch error leads to a difference between D_{15} and D_{16}, allowing the capacitors to be tuned to minimize the error. This mismatch error is represented by the voltage difference (Δ) between V_A and V_B and is directly related to the magnitude of the error.

Fig. 2(a) illustrates the mismatch correction driver, where the nominal capacitor (C_{Nom}) and programmable calibration capacitors (C_{Cal}) are connected in parallel. The control multiplexer (*Ctrl MUX*) manages the switching of the C_{Cal} between the P and N nodes based on inputs from the nominal capacitor code and the calibration code, as illustrated in Fig. 2(b). To adjust the effective capacitance, C_{NOM} and C_{CAL} are switched at the same or different nodes to increase or decrease C_{CAL}. The AND gate controls the calibration capacitance by combining the nominal capacitor switching code from the control MUX with the calibration code. The $D_{Cal,Sign}$ controls the path of the *Ctrl MUX*, while $D_{Cal,Mag}$ adjusts the magnitude of the calibration capacitance. Therefore, this differential structure yields an equivalent $C_{NOM}+C_{CAL}$ or C_{NOM}-C_{CAL} capacitance.

However, previous background calibration [7] requires continuous calibration because the end of the calibration is unknown. To lower power consumption, we need to decrease the update rate, which results in a slower convergence. Furthermore, the CDAC MSB detected error is influenced by the error of the LSB. Consequently, fluctuations in LSB errors cause fluctuations in MSB codes [7], as shown in Fig. 3(a). In contrast, Fig. 3(c) shows the proposed calibration, which starts from the lower bits and sequentially finishes at the upper bits due to completion-aware calibration, resulting in less code variation compared to previous calibrations, as shown in Fig. 3(b). The overall SAR ADC with calibration logic is presented in Fig. 4. The proposed calibration technique differs from the existing method [7] by incorporating a state checker and a state sequencer block. Adding these blocks enables the detection of calibration completion and sequential correction from lower bits.

Fig. 5(a) illustrates the correction process for capacitor mismatch error. C_{eq} represents the equivalent capacitance

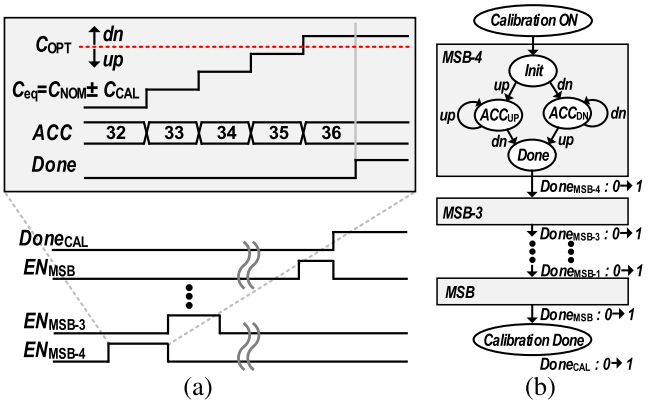

FIGURE 5. Illustration of the proposed calibration; (a) timing diagram of correction and (b) state machine.

TABLE 1. Activation code pattern for calibration.

	$D_{Comp} < 14:8 >$	
Calibration location	Reference [7] (code A / code B)	Proposed (code A / code B)
MSB	0111111 / 1000000	0111111 / 1000000
MSB-1	0011111 / 0100000	x011111 / x100000
MSB-2	0101111 / 0110000	xx01111 / xx10000
MSB-3	0110111 / 0111000	xxx0111 / xxx1000
MSB-4	0111011 / 0111100	xxxx011 / xxxx100

for the current calibration code, $C_{NOM} \pm C_{CAL}$, and it is adjusted to approach the optimal value C_{OPT}. If C_{eq} surpasses the C_{OPT} value, the correction sign reverses, indicating the completion of the corresponding bit calibration. Unlike in reference [7], the proposed method includes a signal, $Done_x$, which indicates the completion of calibration in the bit position. Therefore, the $Done_x$ signal is initialized to 0 and stays high after the calibration completes in the X-bit position. If C_{eq} exceeds C_{OPT}, the sign of Δ changes. This change triggers the $Done_x$ signal to go high, indicating that the calibration for that specific bit has been completed. Fig. 5(b) illustrates the state machine of the correction process. Calibration begins with the MSB-4 bit and continues sequentially. The $Done_x$ signal for each bit triggers the calibration of the next bit. When all bit calibrations are complete, the $Done_{CAL}$ signal is set high, marking the end of the process. Clearing all $Done_x$ will resume the calibration process if we want to rerun the background calibration. Because of the background calibration, this calibration process can be periodically activated to track any variation.

Table 1 presents the pattern table for mismatch detection. The existing detection approach [7] aims to reduce power consumption by comparing multi-bit patterns, thereby lowering activation rates. However, although reducing the activation rate might save power, it comes at the expense of

TABLE 2. Power and calibration activation rate.

	Reference [7]	Proposed	
Calibration location	Activation rate [%]		Power [μW]
MSB	1.5625	1.5625	48.9
MSB-1	1.5625	3.125	47.72
MSB-2	1.5625	6.25	47.03
MSB-3	1.5625	12.5	46.54
MSB-4	1.5625	25	46.12
No calibration	-	-	43

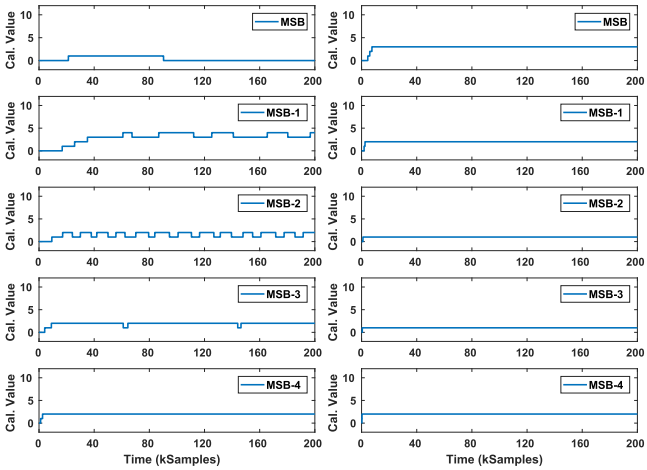

FIGURE 6. Behavioral simulation results of (a) existing [7] and (b) proposed calibration with continuous high amplitude input condition. A sine wave input with a frequency of 211.798kHz and V_{pp} = 700mV. ADC operates at a rate of 2MS/s.

increased correction time. In contrast, the proposed method compares only the necessary minimum bits for detection, including unknown bits, enabling faster calibration without introducing error correlation issues. Table 2 details the power consumption for sample and individual bit calibration conversions. The minimal power consumption is observed when no calibration occurs, while the MSB calibration requires the largest power due to the substantial CDAC capacitance and CDAC driver. The calibration activation rate, assuming random input with equal probability, is summarized in our method based on pattern matching described in Table 1. Extra power is consumed during calibration for clock generation, comparator operation, DAC switching, and logic, as indicated in Table 2. Unlike the previous approach [7] that maintains continuous calibration and requires more comparison bits to reduce activation rates (a 3-bit addition reduces the activation rate by a factor of eight but increases convergence time), our proposed method allows for the deactivation of calibration after coefficient stabilization. The proposed calibration saves power and avoids the trade-off between power efficiency and

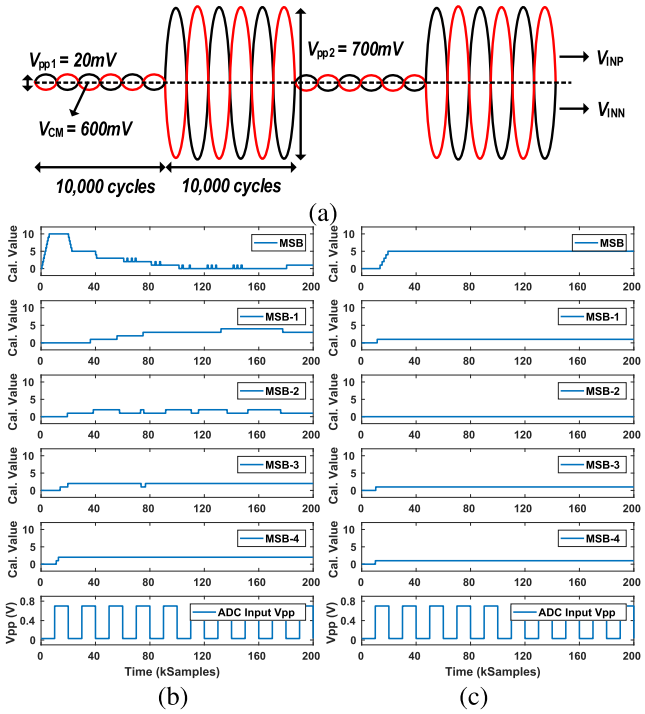

FIGURE 7. Behavioral simulation; (a) input amplitude modulation, (b) existing [7] and (c) proposed simulation results. A sine wave input with a frequency of 211.798kHz is sampled at a rate of 2MS/s, with peak-to-peak voltages of 20mV and 700mV respectively, modulating every 10,000 samples.

calibration speed found in [7], enabling higher activation rates.

C. BEHAVIORAL SIMULATION

Figs. 6(a) and (b) display the behavioral simulation results for the coefficient settling of both the existing [7] and proposed methods. The noise level of the comparator was set to 60 μV_{rms}, and the accumulation value was designated as 1/64. Simulations were conducted using a sine-wave input with a frequency (Fin) of 211.798 kHz and a peak-to-peak voltage (V_{pp}) of 700 mV at a sampling frequency (Fs) of 2 MS/s. In Fig. 6(a), the existing calibration method suffers from continuous fluctuations in calibration coefficients owing to its inability to detect when calibration is complete. Although the lower bit MSB-4 settles early in the calibration process, MSB-3 and higher bits continue to toggle due to comparator noise and other limitations affecting calibration accuracy. The finite correction step results in toggling for MSB-3 and higher bits, even when MSB-4 is already stable, as depicted in Figure 6(a). On the other hand, the proposed method starts at the lower bit position and sequentially corrects the top five MSB CDACs. Consequently, there is no code fluctuation, and the method converges faster than the existing calibration approach, as shown in Figure 6(b).

In [7] approaches, the calibration speed is primarily influenced by the statistics of the input signal. Figure 6 assumes a full-scale input. Under this condition, pattern

TABLE 3. Capacitance of main sampling DACs.

DAC	C_{12}	C_{11}	C_{10}	C_9	C_8	C_7	C_{7r}
Cap. (fF)	1024	512	256	128	64	32	32
DAC	C_6	C_5	C_4	C_{4r}	C_3	C_2	C_1
Cap. (fF)	16	8	4	4	2	1	0.5

TABLE 4. Capacitance of calibration DACs.

Bit / Capacitor	<5>	<4>	<3>	<2>	<1>	<0>
MSB (fF)	8	4	2	1	0.5	0.25
MSB-1 (fF)	8	4	2	1	0.5	0.25
MSB-2 (fF)	-	4	2	1	0.5	0.25
MSB-3 (fF)	-	4	2	1	0.5	0.25
MSB-4 (fF)	-	4	2	1	0.5	0.25

detection for calibrating the top five MSBs occurs frequently, leading to stable calibration coefficient settling. However, initial MSB calibration may be inaccurate if the ADC input signal lacks sufficient statistical randomness. This inaccuracy occurs because the MSB calibration is conducted without verifying the calibration status of the lower-bit CDAC. This scenario is confirmed through behavioral simulation, where the amplitude of the ADC input was periodically modulated with peak-to-peak voltages of 20mV and 700mV for every 10,000 samples in Fig. 7(a). When the input amplitude is small, such as a V_{pp} of 20mV, the pattern detector (as described in Table 1) activates only MSB calibration, leaving the lower CDAC uncalibrated. Although MSB calibration is activated multiple times in this case, its accuracy suffers due to the uncalibrated lower CDAC.

Unlike the existing calibration [7], in the proposed calibration, the MSB calibration waits for the completion of lower-bit calibration for the input amplitude of 20 mV. Once the large input signal with the amplitude of 700 mV arrives, enough lower CDAC calibration patterns happen and complete the calibration within 20k sample cycles, as shown in Fig. 7(c). However, the existing calibration [7] finishes its calibration in 130k sample cycles, marking a significant difference. In practical applications, ADC's conversion accuracy and speed depend not on input statistics. The calibration unit capacitance has a limited correction step of 0.5 LSB. Thus, the convergence value may deviate by $\pm$ 0.5 LSB due to the quantization noise. Due to the sequential calibration from the lower bit position to MSBs, this quantization error is accumulated toward the upper bit calibration code, which makes the final calibration codes in MSB correction differ in Fig. 6 and Fig. 7. However, overall performance, such as signal-to-noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR), are not affected significantly, as shown in Fig. 17. A finer

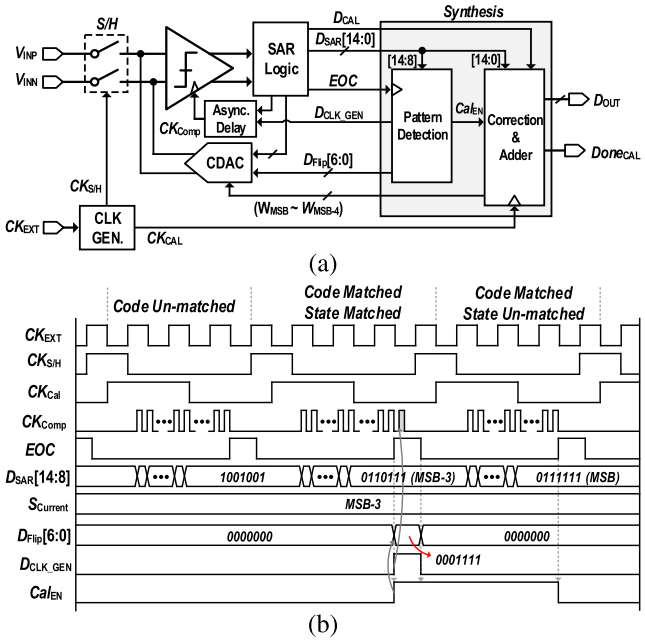

FIGURE 8. Illustration of the (a) overall architecture and (b) timing diagram.

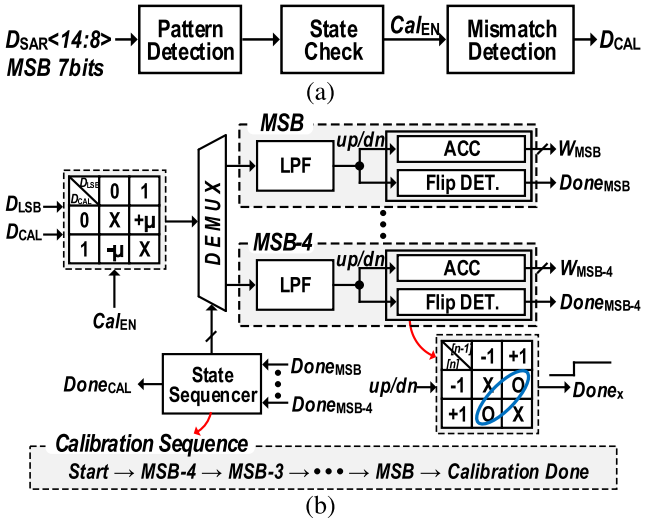

FIGURE 9. Block diagram of the calibration: (a) detection, and (b) correction.

correction step of less than 0.5 LSB is expected to reduce these accumulated quantization noise effects.

III. IMPLEMENTATION

A. ARCHITECTURE AND TIMING

Fig. 8(a) illustrates a simplified block diagram of a SAR ADC implementing calibration. The clock generator produces a sample-and-hold clock ($CK_{S/H}$) and a calibration clock (CK_{CAL}) from an external source. The comparator clock (CK_{Comp}) is asynchronously generated via a resistor ladder-based linear delay cell [16], and it also introduces an additional variable clock for one calibration cycle. Table 3 shows the capacitance of the main DAC that includes two

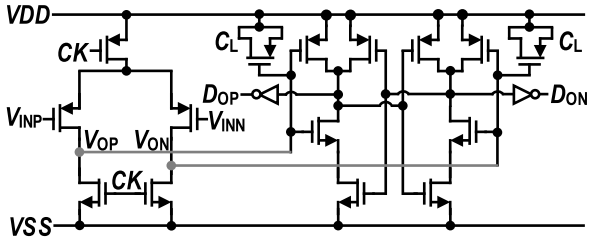

FIGURE 10. Schematic of the two-stage dynamic comparator.

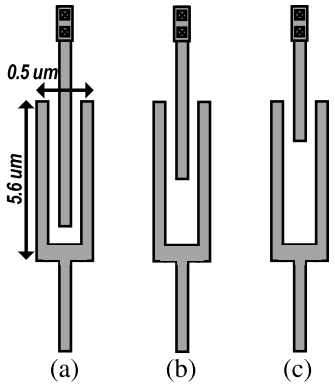

FIGURE 11. Layout of the capacitive DAC; (a) unit layout capacitor of 1 fF, (b) 0.5 fF, and (c) 0.25 fF.

redundancy bits, with the primary redundancy being allocated for mismatch calibration. Table 4 presents the calibration DAC's capacitance. MSB and MSB-1 are composed of six bits each, while MSB-2 through MSB-4 each have five bits, thereby establishing a binary-weighted resolution of $0.5C_{unit}$. The DAC output is operational under a monotonic switching scheme [17].

The digital block includes two types of logic: the pattern detector and the *Correction&Adder* block. The pattern detector logic operates with the end of conversion (EOC) clock signal, while the correction logic operates with CK_{CAL}. Fig. 8(b) depicts the timing diagram for the calibration process. At the rising edge of the EOC clock, the pattern detection logic compares the seven MSB bits (D_{Comp}<14 : 8>) with the calibration activation patterns listed in Table 1. Unlike the previous calibration technique [7], the proposed algorithm introduces additional steps to determine the calibration status.

B. CALIBRATION LOGIC

Fig. 9(a) conceptually illustrates the method used to detect capacitor mismatch. The process involves comparing the seven MSBs, including a redundancy bit, with patterns from a mismatch detection table. This table corrects the five MSB bits identified as having large mismatch errors, as detailed in Table 1. When a detected mismatch pattern bit aligns with the current calibration state bit, the Cal_{EN} signal is activated, satisfying the calibration criteria and initiating the calibration process.

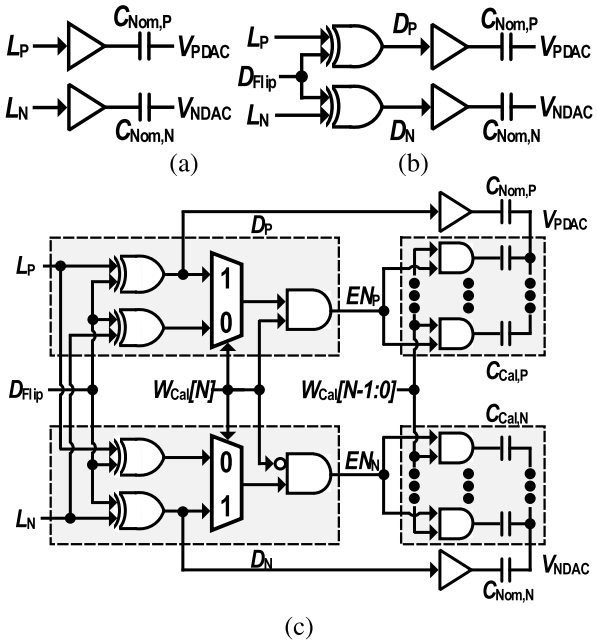

FIGURE 12. CDAC driver of (a) nominal bit, (b) first redundancy bit and (c) calibration bit.

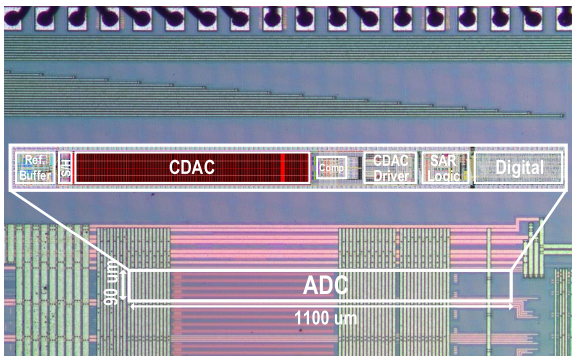

FIGURE 13. Die photograph and layout of the prototype ADC.

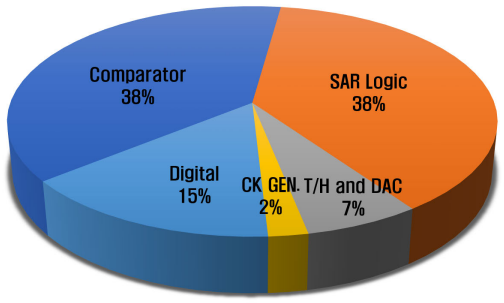

FIGURE 14. Power consumption breakdown of the prototype ADC.

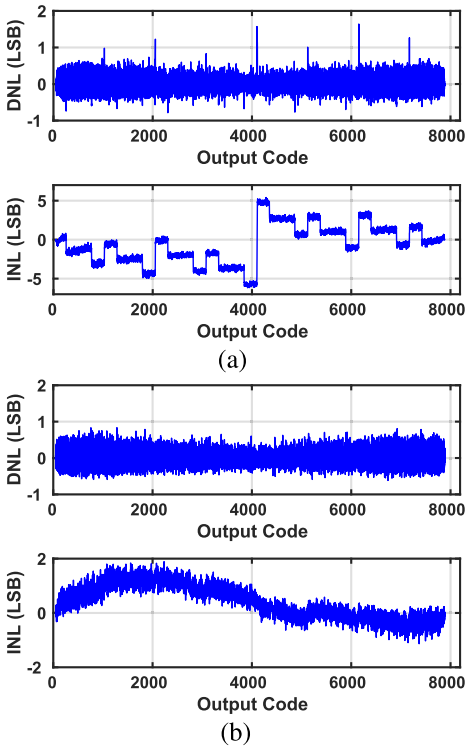

FIGURE 15. Measured DNL/INL performance of the ADC (a) before, and (b) after calibration.

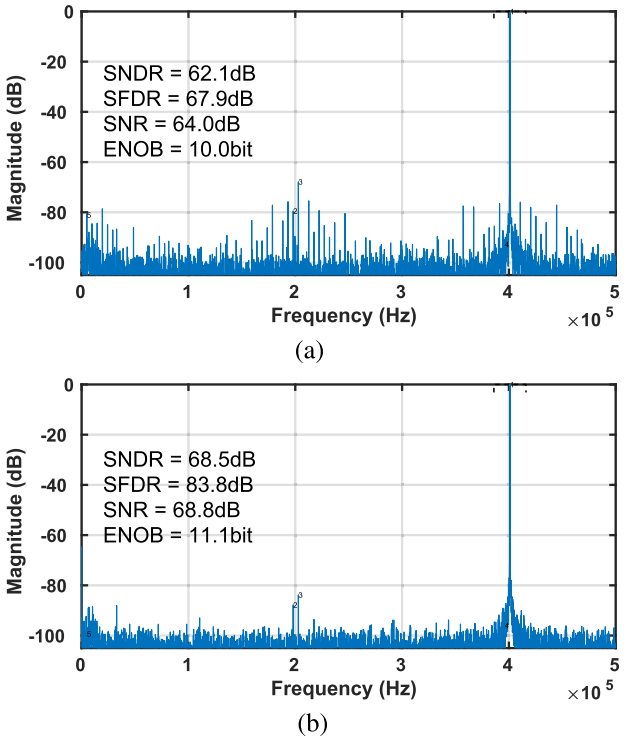

FIGURE 16. Measured spectrum (a) before and (b) after calibration for 400.978 kHz input frequency at 1 MS/s (18,001 points).

Fig. 9(b) depicts the block diagram for the mismatch correction process, which includes several key components: an input correlator, a state sequencer, a DEMUX, and five correction blocks. Each correction block comprises three main elements: a low-pass filter (LPF), an accumulator, and a flip detector. The LPF filters out input noise and provides filtered up/down pulse signals to the accumulator

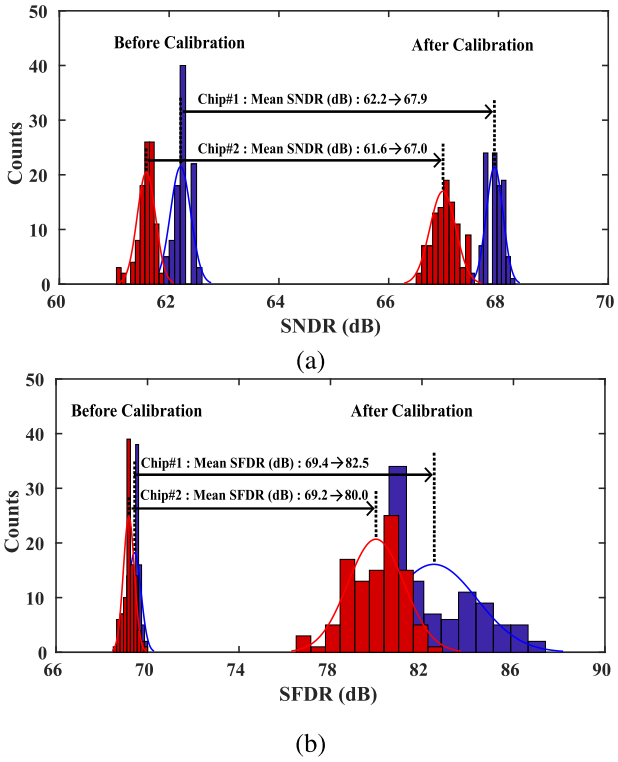

FIGURE 17. Measured (a) SNDR and (b) SFDR histogram with 100 times test for the before and after calibration. Two different chips are measured.

and the flip detector. A majority voting mechanism [18] is employed to implement the LPF for noise filtering. The correlation between D_{LSB} and D_{CAL} indicates the sign of the mismatch. As part of the mismatch correction, the flip detector monitors the up/down pulse signals originating from the LPF to detect when the calibration process is complete. Once the signals have stabilized, this mechanism ensures that the system has reached optimal settings and deactivates any further calibration procedures. Each flip detector generates a $Done_x$ signal, which informs the state sequencer and sets the input for the DEMUX. The accumulator's correction range covers 6 bits from the MSB to MSB-1 and 5 bits from MSB-2 to MSB-4, providing a correction resolution of $0.5C_{unit}$.

C. COMPARATOR

The comparator is a crucial component of power consumption. As illustrated in Fig. 10, the two-stage dynamic comparator consists of a pre-amplifier and a cross-coupled latch stage [18]. The pre-amplifier features a PMOS input pair, reducing input-referred noise. To further enhance the performance of the comparator, MOS capacitors are connected to the V_{OUTP} and V_{OUTN} nodes, minimizing input-referred noise.

D. CDAC DRIVERS

The nominal DAC uses a unit capacitor with a value of 0.5 fF, whereas the calibration capacitor has a unit value of 0.25 fF. The capacitor layout employs a metal-oxide-metal (MoM) structure, utilizing a single metal layer (M5) as depicted in Fig. 11. Even though the default unit capacitor layout is configured for 1 fF, as illustrated in Fig. 11(a), capacitors with values of 0.5 fF and 0.25 fF are also used. These alternative values are depicted in Fig. 11(b) for 0.5 fF and Fig. 11(c) for 0.25 fF. These capacitors are fabricated in varying lengths to compensate for parasitic capacitance, thereby minimizing the total area. Specific nominal and calibration capacitor values can be found in Table 3 and Table 4.

Fig. 12 illustrates three kinds of CDAC drivers: the nominal DAC driver, the redundancy DAC driver, and the calibration DAC driver. Fig. 12(a) shows the nominal DAC driver, which is the simplest among the three and is directly connected from the SAR logic latch output to the DAC buffer input. On the other hand, the redundancy DAC driver, depicted in Fig. 12(b), is engineered to identify and correct mismatches by flipping the CDAC via an XOR gate whenever the D_{Flip} signal is activated. Lastly, as shown in Fig. 12(c), the calibration DAC driver features parallel-connected nominal and programmable correction capacitors to reduce complexity. This configuration allows PADC and NPAC to receive an accumulator value that includes sign bits, eliminating the need to retrieve a distinct correction code from digital logic. Therefore, W_{Cal}[N−1:0] stands for the absolute value of the correction, and $W_{Cal}[N]$ acts as the selection signal for the differential DAC.

IV. MEASUREMENT RESULTS

The die photograph of the implemented SAR ADC, fabricated using a 55-nm ULP CMOS technology, is presented in Fig. 13. The ADC occupies an active area of 0.099 mm^2. Fig. 14 shows the power breakdown of the ADC. To validate the functionality of the calibration, a large capacitor mismatch was intentionally introduced to the CDAC through SPI.

Fig. 15 displays the static performance in terms of DNL and INL. Before calibration, the maximum DNL and INL values were +1.64/−0.78 and +5.41/−6.17 LSB, respectively. After calibration, these values improved to +0.83/−0.62 and +1.89/−1.13 LSB, respectively. However, the mismatch correction capacitance is limited to $0.5C_{unit}$, which inherently restricts the INL performance, accumulating lower residual quantization errors in the upper bits. The improvement in dynamic performance due to calibration is evident in Fig. 16. The FFT spectrum of the ADC was measured at a 1 MS/s sampling rate and a 400.978 kHz sinusoidal input frequency. The calibration process enhanced the third harmonic tone and increased the effective number of bits (ENOB) from 10 bits to 11.1 bits. The signal-to-noise ratio (SNR) also improved from 64.0 dB to 68.8 dB.

Fig. 17 shows histograms of the measured SNDR and SFDR values resulting from 100 repeated calibrations on two different chips, evaluating the calibration process's reliability. The mean SNDR improved from 62.9 dB to 67.9 dB for Chip#1 and from 61.6 dB to 67.0 dB for Chip#2. Similarly, the mean SFDR increased from 69.4 dB to 82.5 dB for

TABLE 5. Performance comparison of SAR ADCs.

	This work	VLSI'15 [6]	JSSC'17 [7]	ASSCC'18 [19]
Technology [nm]	55	14	40	40
Supply voltage [V]	1.2	1.0	1.0	0.7
Sample rate [MS/s]	1.0	70	6.4	1.0
Resolution [bits]	13	12	13	12
Calibration Type	Background	Foreground	Background	Foreground
Calibration-done detection	Yes	Yes	No	Yes
SNDR [dB]	68.5	68.1	64.1	66.54
SFDR [dB]	83.8	80.0	81.9	89.55
ENOB [bit]	11.1	10.89	10.4	10.76
DNL [LSB]	0.83	-	1.08	0.61
INL [LSB]	1.89	-	3.79	0.93
Area [mm^2]	0.099	0.019	0.0675	0.0198
Power [μW]	43	4300	46	2.47
FoM [fJ/conv.-step]	19.59	29.6	5.5	1.43

Chip#1 and from 69.2 dB to 80.0 dB for Chip#2. These results consistently demonstrate an enhancement in both SNDR and SFDR for each chip, confirming the reliability of the calibration process. Table 5 provides a performance comparison of the implemented ADC with other SAR architectures employing calibration methods. Despite utilizing background calibration, the proposed method effectively detects the end of the calibration process and achieves SNDR and SFDR performance comparable to other methods. The prototype ADC operates with a power consumption of 43 μW at a supply voltage of 1.2 V and a 1 MS/s sampling rate.

V. CONCLUSION

This paper has presented a completion-aware background sequential capacitor mismatch calibration technique for SAR ADCs. The proposed method can detect the end of the calibration process, mitigating power consumption associated with calibration and increasing the convergence speed. Moreover, the proposed method can benefit unpredictable input environments, offering significant advantages for various applications. The prototype SAR ADC, fabricated using 55-nm ULP CMOS technology, occupies an active area of 0.099 mm^2. It operates at a sampling rate of 1 MS/s and consumes 43 μW of power from a supply voltage of 1.2 V. These results demonstrate the effectiveness of the proposed method, providing potential for SAR ADC design and implementation in future applications.

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